



H67H2-A3

Rev : 1.0

TABLE OF CONTENTS

| Page | Index |
|------|-----------------------------|
| 1 | COVER PAGE |
| 2 | Block Diagram |
| 3 | GPIO Function Map |
| 4 | CPU - DM/FDI/PEG |
| 5 | CPU - MISC |
| 6 | CPU - DDR3 |
| 7 | CPU - PWR |
| 8 | CPU - GND, CPU_RST_L,VCCSA |
| 9 | DDR3 - CH_A_DIMM1/2 |
| 10 | DDR3 - CH_B_DIMM3/4 |
| 11 | DC/DC VDIMM/DDR_VTT/5VDUAL |
| 12 | PCH - DM/PCI/PE/USB |
| 13 | PCH - SATA |
| 14 | PCH - MISC, Strap Function |
| 15 | PCH - CLK IO, CKG - ICS4180 |
| 16 | PCH - FDI, CLR_CMOS |
| 17 | PCH - PWR |
| 18 | PCH - GND, |
| 19 | Slot - PCI-EX16/PCI-EX1 |
| 20 | Slot - PCI-EX16-2(X4) |
| 21 | USB & SATA - PWR/CONN/HDR |
| 22 | COM, 80 Port, PSUSB |
| 23 | AUDIO ALC892(CHIP) |
| 24 | AUDIO ALC892(PANEL) |
| 25 | PCIE LAN RTL8111E/8105E |

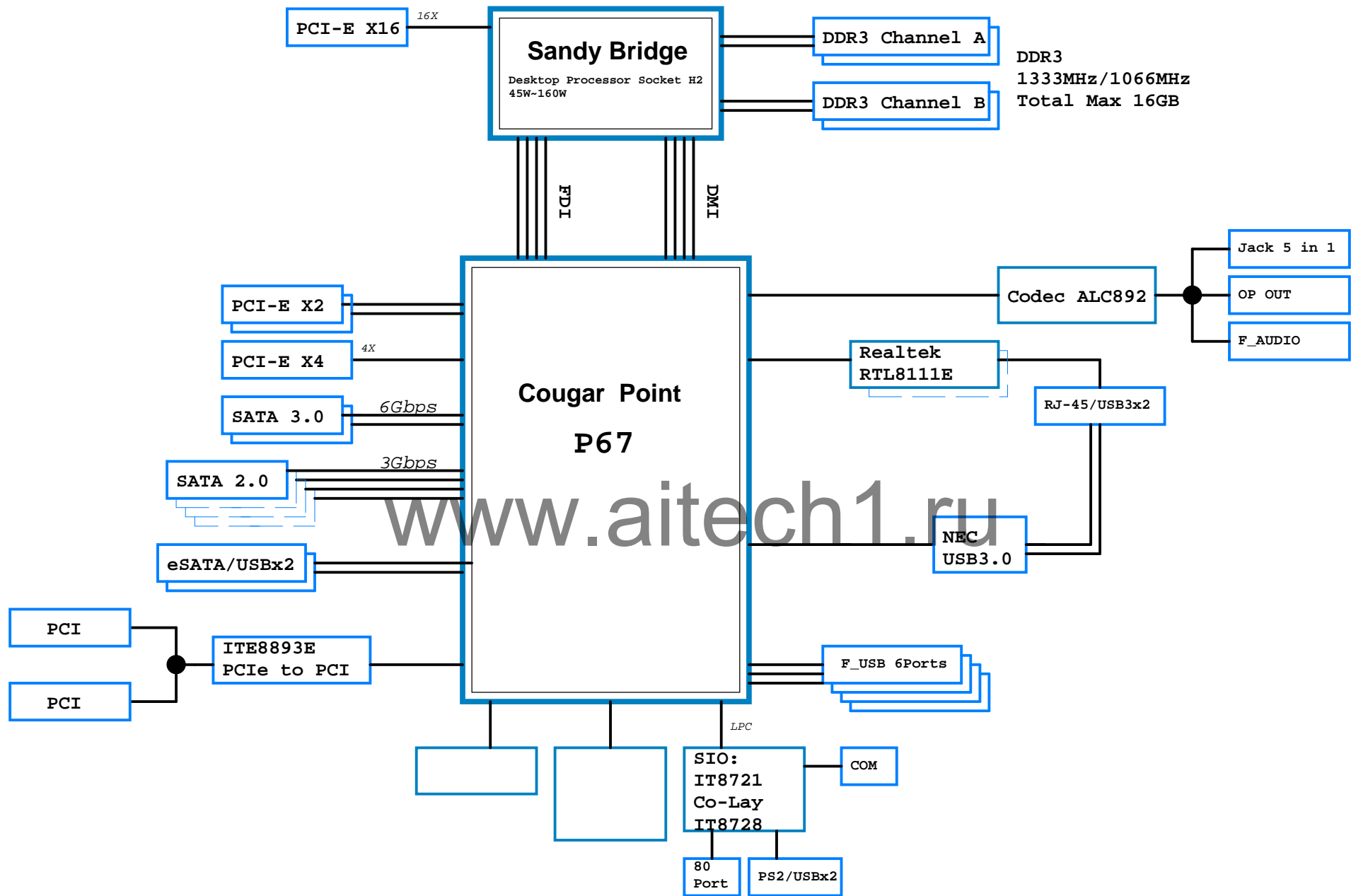
| Page | Index |
|------|-------------------------------|
| 26 | IT8893(PCIE TO PCI) |
| 27 | Slot - PCI1 & PCI2 |
| 28 | USB3.0 Etron EJ168 CONN |
| 29 | SIO-ITE8721/8728 Co-Lay |
| 30 | 104&IMPENDANCE |
| 31 | Front Panel,FAN,PowerConn |
| 32 | RT8121 DC/DC CPUVTT |
| 33 | VCore & VAXG-RT8859A |
| 34 | VCore & VAXG- RT9616 |
| 35 | Power Delivery |
| 36 | Power Sequence, Reset Diagram |
| 37 | Clock Distribution |

REVISION HISTORY:

| Rev | Date | Notes |
|-------|------------|---|
| V.A | 2010/04/16 | Initial version |
| V.B | 2010/06/22 | |
| V.1.0 | 2010/08/09 | |
| V.1.0 | 2010/10/26 | 由P67h2-a3-0921-bom chang PCH--H67 DEL USB3.0&USB3.0-ESD CHANG USB2LAN RT8859A---->RT8859M |

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NOTE:
Design by 428971_428971_Sugar_Bay_and_BromolowWS_PDG_Rev_0_8.pdf,
428880_428880_Cougar_Point_Desktop_Ballout_Mech_Package_Rev1p0.zip



3PIO function

| Pin Name | Power Well | Usage | Default Status |
|----------|------------|------------------|----------------|
| GPIO0 | VCC3 | FP_AUD_DETECT | GPI |
| GPIO1 | VCC3 | GP1_BOMDET2 | GPI |
| GPIO6 | VCC3 | GP6_BOMDET3 | GPI |
| GPIO7 | VCC3 | GP6_BOMDET4 | GPI |
| GPIO9 | 3VSB | USB_OC_L5 | Native |
| GPIO10 | 3VSB | USB_OC_L6 | Native |
| GPIO11 | 3VSB | GP6_BOMDET4 | Native |
| GPIO12 | 3VSB | GP6_BOMDET4 | Native |
| GPIO13 | 3VSB | GP6_BOMDET4 | GPI |
| GPIO14 | 3VSB | USB_OC_L7 | Native |
| GPIO16 | VCC3 | Reserve for TPM | GPI |
| GPIO17 | VCC3 | GP17_BOMDET1 | GPI |
| GPIO21 | VCC3 | GPIO21_COM2_DET | GPI |
| GPIO22 | VCC3 | CLR_CMOS_GP22 | GPI |
| GPIO24 | 3VSB | PCH_SKTOCC_L | GPO |
| GPIO34 | VCC3 | GPIO34_TCM_PST_L | GPI |
| GPIO38 | VCC3 | GPIO38_TCM | GPI |
| GPIO39 | VCC3 | GPIO39_CASE0 | GPI |
| GPIO40 | 3VSB | USB_OC_L1 | Native |
| GPIO41 | 3VSB | USB_OC_L2 | Native |
| GPIO42 | 3VSB | USB_OC_L3 | Native |
| GPIO43 | 3VSB | USB_OC_L4 | Native |
| GPIO48 | VCC3 | GPIO48_CASE1 | GPI |
| GPIO49 | VCC3 | Reserve for TPM | GPI |
| GPIO59 | 3VSB | USB_OC_L0 | Native |
| GPIO68 | VCC3 | GPIO68_USBDDET1 | GPI |
| GPIO69 | VCC3 | GPIO69_USBDDET2 | GPI |
| GPIO70 | VCC3 | GPIO70_USBDDET3 | Native |
| GPIO71 | VCC3 | Reserve for TPM | Native |
| GPIO72 | 3VSB | GPIO72_BOMDET5 | Native |

SIO-GPIO function

| Pin Name | Power Well | Usage | Default Status |
|----------|------------|---------------|----------------|
| GP16 | | SIO_BEEP | |
| GP23 | | Power LED | |
| GP22 | | Power LED | |
| GP52 | | FAN_TAC2 | |
| GP51 | | FAN_CTL2 | |
| GP37 | | FAN_TAC3 | |
| GP36 | | FAN_CTL3 | |
| GP30 | | 8723_ATXPWRGD | |
| GP26 | | COM | |
| GP27 | | COM | |
| GP24 | | COM | |
| GP25 | | COM | |
| GP21 | | COM | |
| GP20 | | COM | |
| GP17 | | COM | |
| GP12 | | SIO_PCIRST1_L | |
| GP11 | | SIO_PCIRST2_L | |
| GP14 | | PWRGD1 | |
| GP62 | | KBRST_L | |
| GP44 | | SIO_PWRBTN_L | |
| GP54 | | LPC_PME_L | |
| GP43 | | FP_PWRBTN_L | |
| GP42 | | SIO_PSON_L | |
| GP17 | | COM | |
| GP56 | | MCLK | |
| GP57 | | MDATA | |
| GP60 | | KCLK | |
| GP61 | | KDATA | |
| GP10 | | SIO_PCIRST3_L | |
| GP55 | | RSMRST_R_L | |

PCH Strap Pin

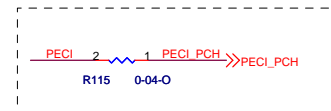
| Pin Name | Usage | Default Status |
|------------------|--|--|
| SPKR | No Reboot | 20K internal pull-down · No Reboot Mode with TCO Disabled: |
| INIT3_3V# | Reserved | 20K internal pull-up · intend for Firmware Hub. |
| GNT[3]#/GPIO[55] | Disable Top-Block Swap | 20K internal pull-up · "topblock swap" mode Disable |
| INTVRMEN | Enable Integrated 1.05V VRM | Need External Pull-up · Integrated 1.05V VRM Enable |
| GNT1# / GPIO51 | Boot BIOS Strap bit [1] BBS[1] | 20K internal pull-up · The default flash selection is the SPI flash.All |
| SATA1GP / GPIO19 | Boot BIOS Strap bit[0] BBS[0] | 20K internal pull-up · The default flash selection is the SPI flash.All |
| HDA_SDO | Flash Descriptor Security Override/ ME | Internal pull-down. The security measures defined in the Flash Descriptor will be in effect(default) |
| DF_TV5 | Enable DMI termination voltage | This signal has a weak internal pull-down. |
| GPIO28 | Eable On-Die PLL Voltage Regulator | The On-Die PLL voltage regulator is enabled |
| HDA_SYNC | On-Die PLL Voltage Regulator Voltage Select 1.8V | 20K internal pull-down.On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low. |
| GPIO15 | Enable TLS Confidentiality | Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. |

Table 7-1. Power On Strapping Options

| | Symbol | Strapping Event | Value | Description |
|------------------|--------------|-------------------------|-------|--|
| JP2 | Flashseg1_EN | Internal VCC-OK/LRESET# | 1 | Disable |
| Pin 122 | | | 0 | Enable Flash I/F Address Segment FFF8_0000 ~ FFFF_FFFF & 000E_0000 ~ 000F_FFFF |
| JP4 | K8PWR_EN | Internal VCC-OK | 1 | Disable K8 power sequence function |
| Pin 126 | | | 0 | Enable K8 power sequence function |
| [JP3,JP5] | FAN_CTL_SE L | Internal VCC-OK | 11 | The default value of EC Index 63h/6Bh/73h is 80h. |
| Pin 124 & Pin 46 | | | 10 | The default value of EC Index 63h/6Bh/73h is FFh. |
| | | | 01 | The default value of EC Index 63h/6Bh/73h is 00h. |
| | | | 00 | The default value of EC Index 63h/6Bh/73h is 40h. |

Elitegroup Computer Systems

| | | | |
|----------------------|--------------------------|-------|---------|
| Title | | | |
| 30-GPIO Function Map | | | |
| Size Custom | Document Number | | Rev |
| | H67H2-A3 | | 1.0 |
| Date: | Friday, October 29, 2010 | Sheet | 3 of 37 |



| | |
|-------------------|-------------------|
| 9 M_DATA_A[0..63] | ← M_DATA A[0..63] |
| 9 M_DQS_A_P[0..7] | ← M_DQS A P[0..7] |
| 9 M_DQS_A_N[0..7] | ← M_DQS A N[0..7] |
| 9 M_MA_A[0..15] | ← M_MA A[0..15] |
| 9 M_BS_A[0..2] | ← M_BS A[0..2] |
| 9 M_CS_A_L[0..3] | ← M_CS A L[0..3] |
| 9 M_CKE_A[0..3] | ← M_CKE A[0..3] |
| 9 M_ODT_A[0..3] | ← M_ODT A[0..3] |
| 9 M_CLK_A_P[0..3] | ← M_CLK A P[0..3] |
| 9 M_CLK_A_N[0..3] | ← M_CLK A N[0..3] |
| 9 M_WE_A_L | ← M_WE A L |
| 9 M_CAS_A_L | ← M_CAS A L |
| 9 M_RAS_A_L | ← M_RAS A L |

DDR3 CH.A

9,10 DDR3_DRAMRST_L ← DDR3_DRAMRST_L

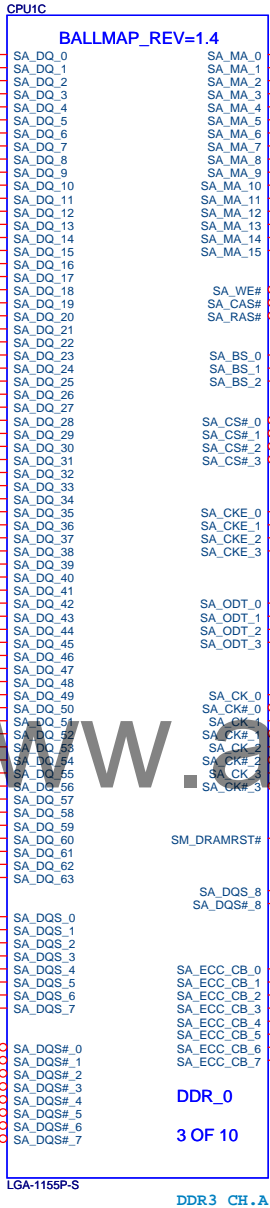
| | |
|--------------------|-------------------|
| 10 M_DATA_B[0..63] | ← M_DATA B[0..63] |
| 10 M_DQS_B_P[0..7] | ← M_DQS B P[0..7] |
| 10 M_DQS_B_N[0..7] | ← M_DQS B N[0..7] |
| 10 M_MA_B[0..15] | ← M_MA B[0..15] |
| 10 M_BS_B[0..2] | ← M_BS B[0..2] |
| 10 M_CS_B_L[0..3] | ← M_CS B L[0..3] |
| 10 M_CKE_B[0..3] | ← M_CKE B[0..3] |
| 10 M_ODT_B[0..3] | ← M_ODT B[0..3] |
| 10 M_CLK_B_P[0..3] | ← M_CLK B P[0..3] |
| 10 M_CLK_B_N[0..3] | ← M_CLK B N[0..3] |
| 10 M_WE_B_L | ← M_WE B L |
| 10 M_CAS_B_L | ← M_CAS B L |
| 10 M_RAS_B_L | ← M_RAS B L |

DDR3 CH.B

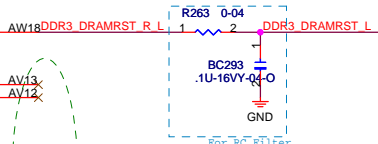
| | | |
|------------|------|----------|
| M_DATA_A0 | AJ3 | SA_DQ_0 |
| M_DATA_A1 | AJ4 | SA_DQ_1 |
| M_DATA_A2 | AL3 | SA_DQ_2 |
| M_DATA_A3 | AL4 | SA_DQ_3 |
| M_DATA_A4 | AJ2 | SA_MA_4 |
| M_DATA_A5 | AL1 | SA_MA_5 |
| M_DATA_A6 | AL2 | SA_MA_6 |
| M_DATA_A7 | AL1 | SA_MA_7 |
| M_DATA_A8 | AN1 | SA_MA_8 |
| M_DATA_A9 | AN4 | SA_MA_9 |
| M_DATA_A10 | AR3 | SA_MA_10 |
| M_DATA_A11 | AR4 | SA_MA_11 |
| M_DATA_A12 | AN2 | SA_MA_12 |
| M_DATA_A13 | AR2 | SA_MA_13 |
| M_DATA_A14 | AR2 | SA_MA_14 |
| M_DATA_A15 | AR1 | SA_MA_15 |
| M_DATA_A16 | AV2 | SA_DQ_16 |
| M_DATA_A17 | AW3 | SA_DQ_17 |
| M_DATA_A18 | AV5 | SA_DQ_18 |
| M_DATA_A19 | AU2 | SA_DQ_19 |
| M_DATA_A20 | AU3 | SA_DQ_20 |
| M_DATA_A21 | AU3 | SA_DQ_21 |
| M_DATA_A22 | AU5 | SA_DQ_22 |
| M_DATA_A23 | AV5 | SA_DQ_23 |
| M_DATA_A24 | AV7 | SA_DQ_24 |
| M_DATA_A25 | AU7 | SA_DQ_25 |
| M_DATA_A26 | AV9 | SA_DQ_26 |
| M_DATA_A27 | AU9 | SA_DQ_27 |
| M_DATA_A28 | AV7 | SA_DQ_28 |
| M_DATA_A29 | AW7 | SA_DQ_29 |
| M_DATA_A30 | AU7 | SA_DQ_30 |
| M_DATA_A31 | AY9 | SA_DQ_31 |
| M_DATA_A32 | AU35 | SA_DQ_32 |
| M_DATA_A33 | AW37 | SA_DQ_33 |
| M_DATA_A34 | AU39 | SA_DQ_34 |
| M_DATA_A35 | AW35 | SA_DQ_35 |
| M_DATA_A37 | AY36 | SA_DQ_36 |
| M_DATA_A38 | AU38 | SA_DQ_37 |
| M_DATA_A39 | AU37 | SA_DQ_38 |
| M_DATA_A40 | AR37 | SA_DQ_39 |
| M_DATA_A41 | AR37 | SA_DQ_40 |
| M_DATA_A42 | AN35 | SA_DQ_41 |
| M_DATA_A43 | AN37 | SA_DQ_42 |
| M_DATA_A44 | AR39 | SA_DQ_43 |
| M_DATA_A45 | AR38 | SA_DQ_44 |
| M_DATA_A46 | AN39 | SA_DQ_45 |
| M_DATA_A47 | AN40 | SA_DQ_46 |
| M_DATA_A48 | AL40 | SA_DQ_47 |
| M_DATA_A49 | AL37 | SA_DQ_48 |
| M_DATA_A50 | AJ38 | SA_DQ_49 |
| M_DATA_A51 | AJ37 | SA_DQ_50 |
| M_DATA_A52 | AJ38 | SA_DQ_51 |
| M_DATA_A53 | AJ38 | SA_DQ_52 |
| M_DATA_A54 | AJ39 | SA_DQ_53 |
| M_DATA_A55 | AJ40 | SA_DQ_54 |
| M_DATA_A56 | AG40 | SA_DQ_55 |
| M_DATA_A57 | AG37 | SA_DQ_56 |
| M_DATA_A58 | AE38 | SA_DQ_57 |
| M_DATA_A59 | AE37 | SA_DQ_58 |
| M_DATA_A60 | AG39 | SA_DQ_59 |
| M_DATA_A61 | AG38 | SA_DQ_60 |
| M_DATA_A62 | AE39 | SA_DQ_61 |
| M_DATA_A63 | AE40 | SA_DQ_62 |

| | | |
|------------|------|----------|
| M_DQS_A_P0 | AK3 | SA_DQS_0 |
| M_DQS_A_P1 | AP3 | SA_DQS_1 |
| M_DQS_A_P2 | AW4 | SA_DQS_2 |
| M_DQS_A_P3 | AV8 | SA_DQS_3 |
| M_DQS_A_P4 | AV37 | SA_DQS_4 |
| M_DQS_A_P5 | AP38 | SA_DQS_5 |
| M_DQS_A_P6 | AK38 | SA_DQS_6 |
| M_DQS_A_P7 | AF38 | SA_DQS_7 |

| | | |
|------------|------|-----------|
| M_DQS_A_N0 | AK2 | SA_DQS#_0 |
| M_DQS_A_N1 | AP2 | SA_DQS#_1 |
| M_DQS_A_N2 | AV4 | SA_DQS#_2 |
| M_DQS_A_N3 | AW8 | SA_DQS#_3 |
| M_DQS_A_N4 | AV39 | SA_DQS#_4 |
| M_DQS_A_N5 | AP39 | SA_DQS#_5 |
| M_DQS_A_N6 | AK39 | SA_DQS#_6 |
| M_DQS_A_N7 | AF39 | SA_DQS#_7 |



| | |
|------|------------|
| AV27 | M_MA_A0 |
| AV24 | M_MA_A1 |
| AW24 | M_MA_A2 |
| AW23 | M_MA_A3 |
| AW24 | M_MA_A4 |
| AT24 | M_MA_A5 |
| AT23 | M_MA_A6 |
| AJ22 | M_MA_A7 |
| AV22 | M_MA_A8 |
| AT22 | M_MA_A9 |
| AV28 | M_MA_A10 |
| AJ21 | M_MA_A11 |
| AT21 | M_MA_A12 |
| AW22 | M_MA_A13 |
| AJ20 | M_MA_A14 |
| AT20 | M_MA_A15 |
| AW29 | M_WE_A_L |
| AW30 | M_CAS_A_L |
| AJ28 | M_RAS_A_L |
| AV29 | M_BS_A0 |
| AW28 | M_BS_A1 |
| AV20 | M_BS_A2 |
| AJ29 | M_CS_A_L0 |
| AW30 | M_CS_A_L1 |
| AJ33 | M_CS_A_L2 |
| AJ33 | M_CS_A_L3 |
| AV19 | M_CKE_A0 |
| AT19 | M_CKE_A1 |
| AJ18 | M_CKE_A2 |
| AV18 | M_CKE_A3 |
| AV31 | M_ODT_A0 |
| AJ32 | M_ODT_A1 |
| AJ30 | M_ODT_A2 |
| AW33 | M_ODT_A3 |
| AY25 | M_CLK_A_P0 |
| AW25 | M_CLK_A_N0 |
| AJ24 | M_CLK_A_P1 |
| AY25 | M_CLK_A_N1 |
| AY27 | M_CLK_A_N2 |
| AV26 | M_CLK_A_P3 |
| AW26 | M_CLK_A_N3 |



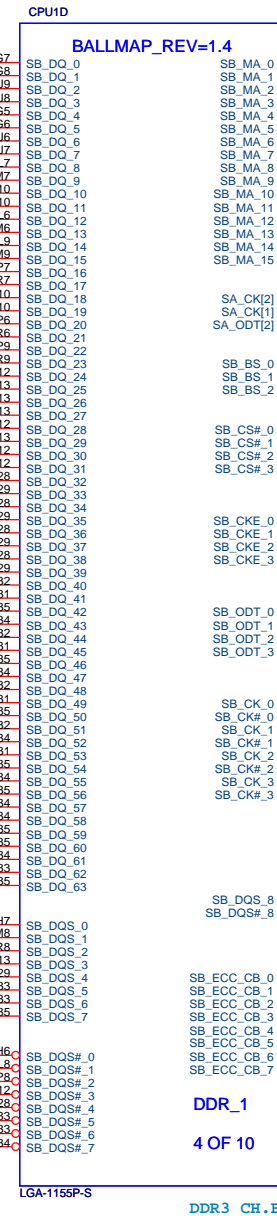
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|------|---------|
| AV13 | M_MA_A0 |
| AV12 | M_MA_A1 |
| AJ12 | M_MA_A2 |
| AJ14 | M_MA_A3 |
| AW13 | M_MA_A4 |
| AY13 | M_MA_A5 |
| AJ13 | M_MA_A6 |
| AJ15 | M_MA_A7 |
| AY12 | M_MA_A8 |
| AW12 | M_MA_A9 |

Pay Attention to This Part!

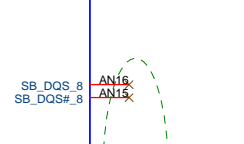
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| M_DATA_B0 | AG7 | SB_DQ_0 |
| M_DATA_B1 | AG8 | SB_DQ_1 |
| M_DATA_B2 | AJ8 | SB_DQ_2 |
| M_DATA_B3 | AG5 | SB_DQ_3 |
| M_DATA_B4 | AG6 | SB_DQ_4 |
| M_DATA_B5 | AJ6 | SB_DQ_5 |
| M_DATA_B6 | AJ7 | SB_DQ_6 |
| M_DATA_B7 | AL7 | SB_DQ_7 |
| M_DATA_B8 | AM7 | SB_DQ_8 |
| M_DATA_B9 | AM7 | SB_DQ_9 |
| M_DATA_B10 | AM10 | SB_DQ_10 |
| M_DATA_B11 | AL10 | SB_DQ_11 |
| M_DATA_B12 | AL6 | SB_DQ_12 |
| M_DATA_B13 | AL9 | SB_DQ_13 |
| M_DATA_B14 | AL9 | SB_DQ_14 |
| M_DATA_B15 | AM9 | SB_DQ_15 |
| M_DATA_B16 | AP7 | SB_DQ_16 |
| M_DATA_B17 | AR7 | SB_DQ_17 |
| M_DATA_B18 | AP10 | SB_DQ_18 |
| M_DATA_B19 | AR10 | SB_DQ_19 |
| M_DATA_B20 | AP6 | SB_DQ_20 |
| M_DATA_B21 | AR6 | SB_DQ_21 |
| M_DATA_B22 | AP9 | SB_DQ_22 |
| M_DATA_B23 | AR9 | SB_DQ_23 |
| M_DATA_B24 | AM12 | SB_DQ_24 |
| M_DATA_B25 | AM13 | SB_DQ_25 |
| M_DATA_B26 | AR13 | SB_DQ_26 |
| M_DATA_B27 | AP13 | SB_DQ_27 |
| M_DATA_B28 | AL12 | SB_DQ_28 |
| M_DATA_B29 | AL13 | SB_DQ_29 |
| M_DATA_B30 | AL13 | SB_DQ_30 |
| M_DATA_B31 | AP12 | SB_DQ_31 |
| M_DATA_B32 | AR28 | SB_DQ_32 |
| M_DATA_B33 | AR29 | SB_DQ_33 |
| M_DATA_B34 | AL28 | SB_DQ_34 |
| M_DATA_B35 | AL29 | SB_DQ_35 |
| M_DATA_B36 | AP28 | SB_DQ_36 |
| M_DATA_B37 | AP29 | SB_DQ_37 |
| M_DATA_B38 | AM28 | SB_DQ_38 |
| M_DATA_B39 | AM29 | SB_DQ_39 |
| M_DATA_B40 | AP32 | SB_DQ_40 |
| M_DATA_B41 | AP31 | SB_DQ_41 |
| M_DATA_B42 | AP35 | SB_DQ_42 |
| M_DATA_B43 | AP34 | SB_DQ_43 |
| M_DATA_B44 | AR32 | SB_DQ_44 |
| M_DATA_B45 | AR31 | SB_DQ_45 |
| M_DATA_B46 | AR35 | SB_DQ_46 |
| M_DATA_B47 | AR34 | SB_DQ_47 |
| M_DATA_B48 | AM32 | SB_DQ_48 |
| M_DATA_B49 | AM31 | SB_DQ_49 |
| M_DATA_B50 | AL35 | SB_DQ_50 |
| M_DATA_B51 | AL32 | SB_DQ_51 |
| M_DATA_B52 | AM34 | SB_DQ_52 |
| M_DATA_B53 | AM35 | SB_DQ_53 |
| M_DATA_B54 | AL34 | SB_DQ_54 |
| M_DATA_B55 | AL34 | SB_DQ_55 |
| M_DATA_B56 | AH35 | SB_DQ_56 |
| M_DATA_B57 | AH34 | SB_DQ_57 |
| M_DATA_B58 | AE34 | SB_DQ_58 |
| M_DATA_B59 | AE35 | SB_DQ_59 |
| M_DATA_B60 | AJ35 | SB_DQ_60 |
| M_DATA_B61 | AJ34 | SB_DQ_61 |
| M_DATA_B62 | AF33 | SB_DQ_62 |
| M_DATA_B63 | AF35 | SB_DQ_63 |

| | | |
|------------|------|----------|
| M_DQS_B_P0 | AH7 | SB_DQS_0 |
| M_DQS_B_P1 | AM8 | SB_DQS_1 |
| M_DQS_B_P2 | AR8 | SB_DQS_2 |
| M_DQS_B_P3 | AN13 | SB_DQS_3 |
| M_DQS_B_P4 | AN13 | SB_DQS_4 |
| M_DQS_B_P5 | AP33 | SB_DQS_5 |
| M_DQS_B_P6 | AL33 | SB_DQS_6 |
| M_DQS_B_P7 | AG35 | SB_DQS_7 |

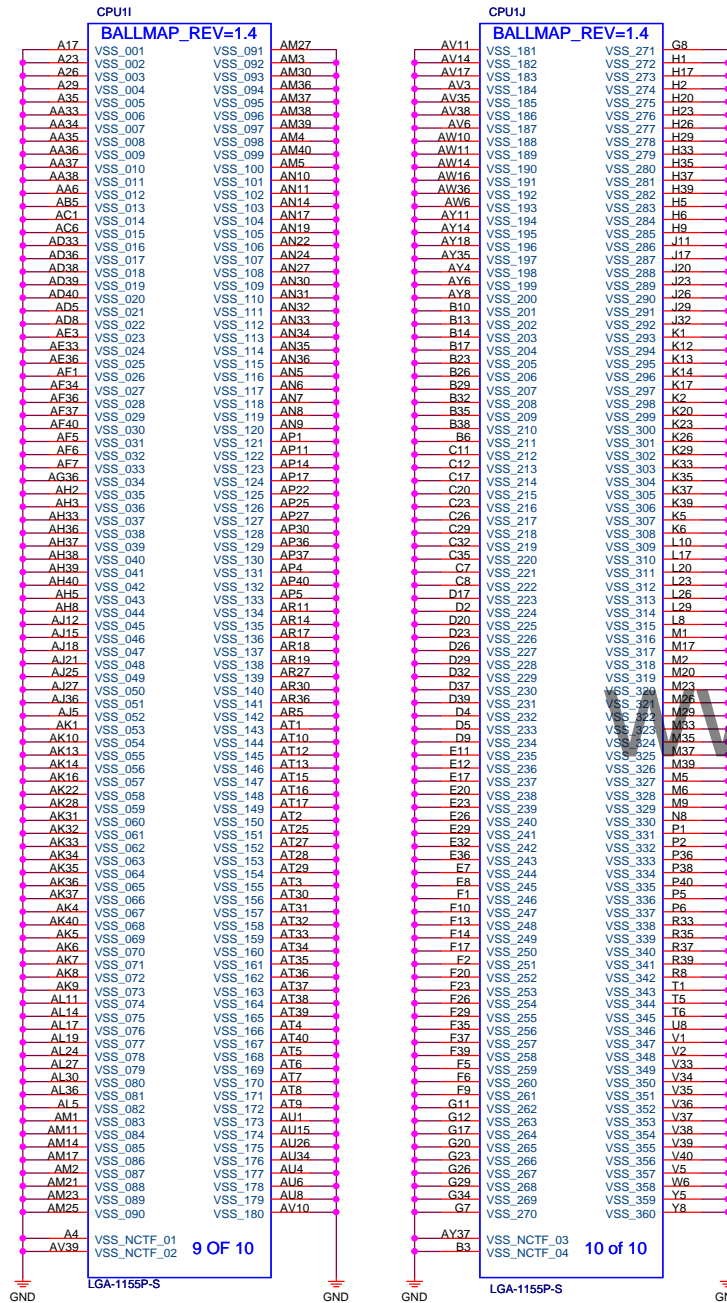
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|------------|------|-----------|
| M_DQS_B_N0 | AH6 | SB_DQS#_0 |
| M_DQS_B_N1 | AL8 | SB_DQS#_1 |
| M_DQS_B_N2 | AP8 | SB_DQS#_2 |
| M_DQS_B_N3 | AN12 | SB_DQS#_3 |
| M_DQS_B_N4 | AN28 | SB_DQS#_4 |
| M_DQS_B_N5 | AR33 | SB_DQS#_5 |
| M_DQS_B_N6 | AM33 | SB_DQS#_6 |
| M_DQS_B_N7 | AG34 | SB_DQS#_7 |



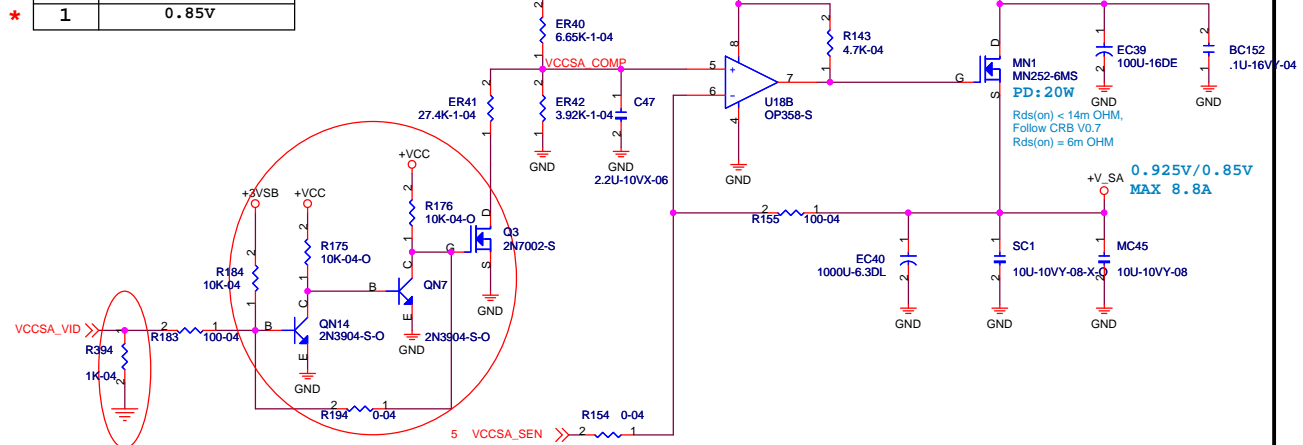
| | |
|------|------------|
| AK24 | M_MA_B0 |
| AM20 | M_MA_B1 |
| AM19 | M_MA_B2 |
| AK18 | M_MA_B3 |
| AP19 | M_MA_B4 |
| AP18 | M_MA_B5 |
| AM18 | M_MA_B6 |
| AL18 | M_MA_B7 |
| AN18 | M_MA_B8 |
| AY17 | M_MA_B9 |
| AN23 | M_MA_B10 |
| AJ17 | M_MA_B11 |
| AT18 | M_MA_B12 |
| AR26 | M_MA_B13 |
| AY16 | M_MA_B14 |
| AV16 | M_MA_B15 |
| AR25 | M_WE_B_L |
| AK25 | M_CAS_B_L |
| AP24 | M_RAS_B_L |
| AP23 | M_BS_B0 |
| AM24 | M_BS_B1 |
| AW17 | M_BS_B2 |
| AN25 | M_CS_B_L0 |
| AN26 | M_CS_B_L1 |
| AT25 | M_CS_B_L2 |
| AT26 | M_CS_B_L3 |
| AU16 | M_CKE_B0 |
| AY15 | M_CKE_B1 |
| AW15 | M_CKE_B2 |
| AV15 | M_CKE_B3 |
| AL26 | M_ODT_B0 |
| AP26 | M_ODT_B1 |
| AK26 | M_ODT_B2 |
| AK26 | M_ODT_B3 |
| AL21 | M_CLK_B_P0 |
| AL22 | M_CLK_B_N0 |
| AL20 | M_CLK_B_P1 |
| AK20 | M_CLK_B_N1 |
| AL23 | M_CLK_B_P2 |
| AM22 | M_CLK_B_N2 |
| AP21 | M_CLK_B_P3 |
| AN21 | M_CLK_B_N3 |



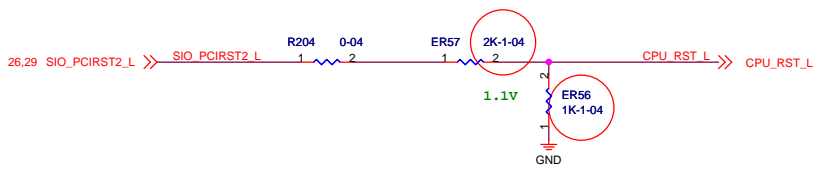
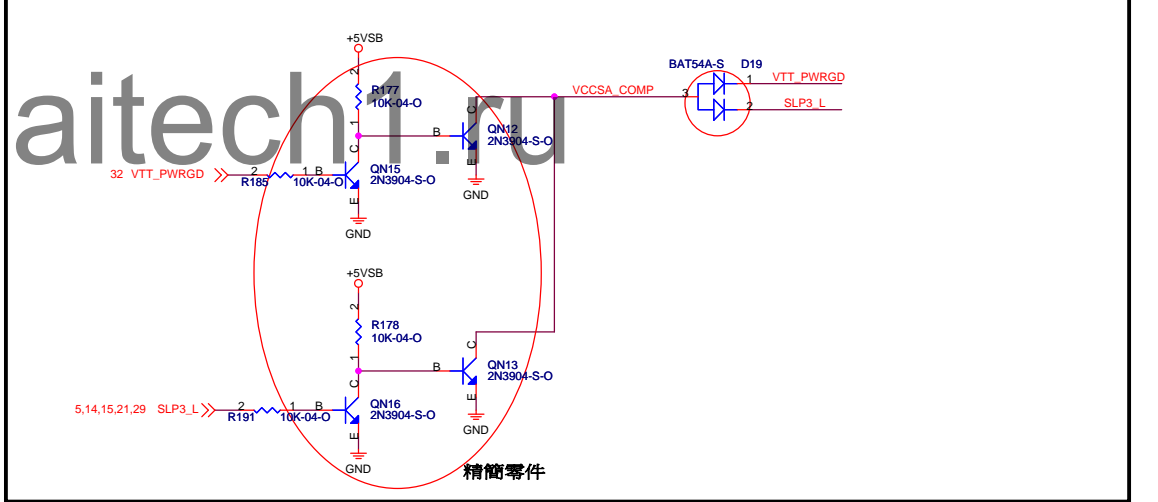
| | |
|------|---------|
| AL16 | M_MA_B0 |
| AM16 | M_MA_B1 |
| AP16 | M_MA_B2 |
| AR16 | M_MA_B3 |
| AL15 | M_MA_B4 |
| AM15 | M_MA_B5 |
| AR15 | M_MA_B6 |
| AL15 | M_MA_B7 |

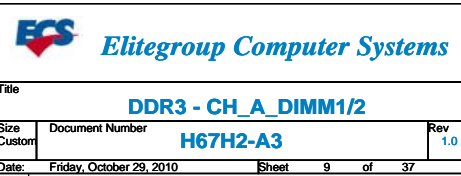


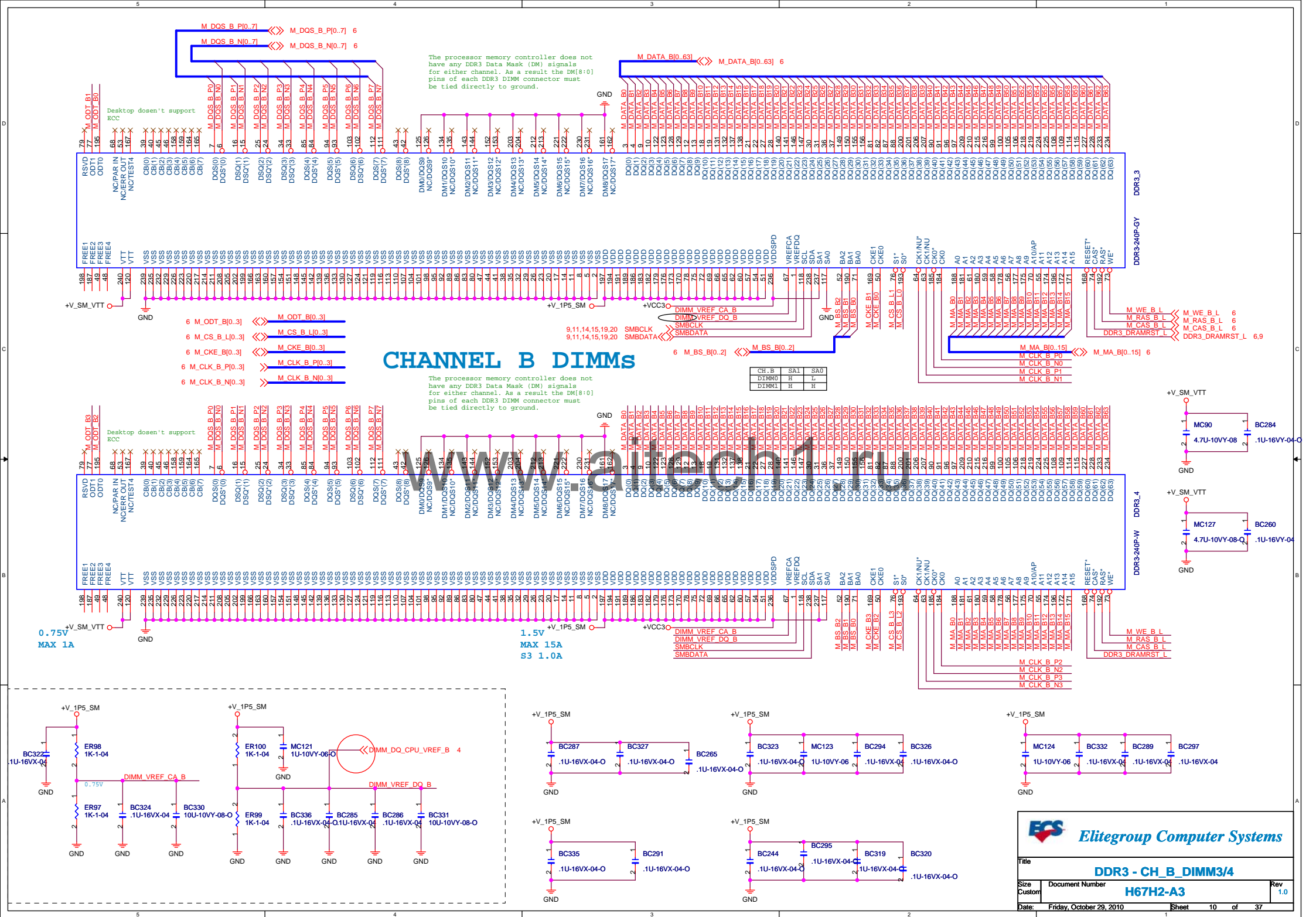
| VCCSA voltage selection | |
|-------------------------|--------|
| VID | +V_SA |
| 0 | 0.925V |
| 1 | 0.85V |

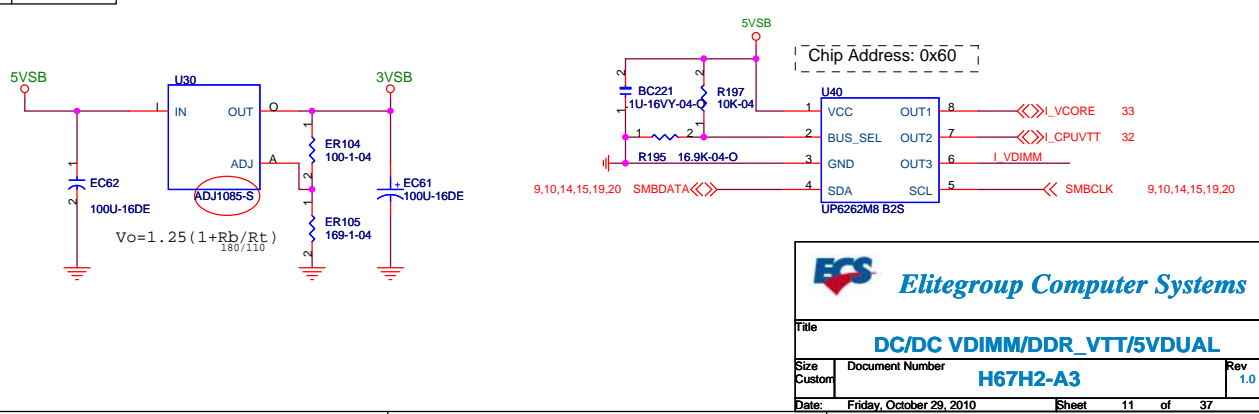
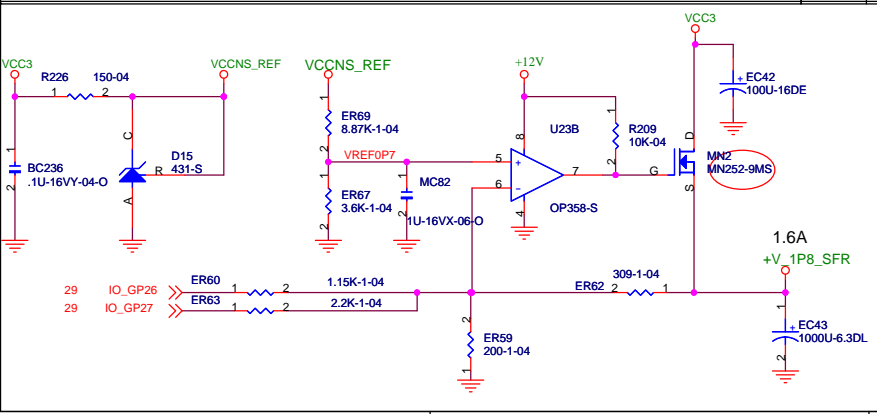
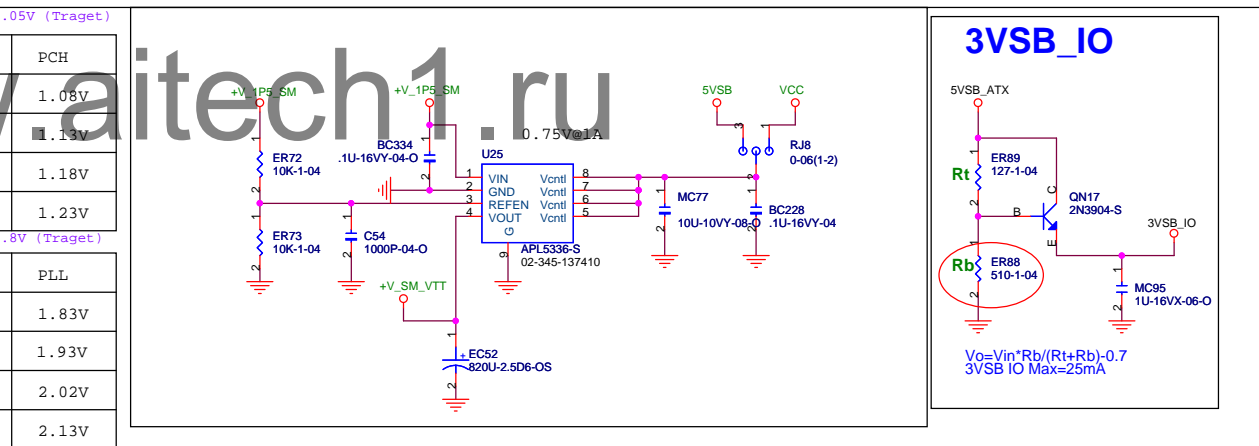
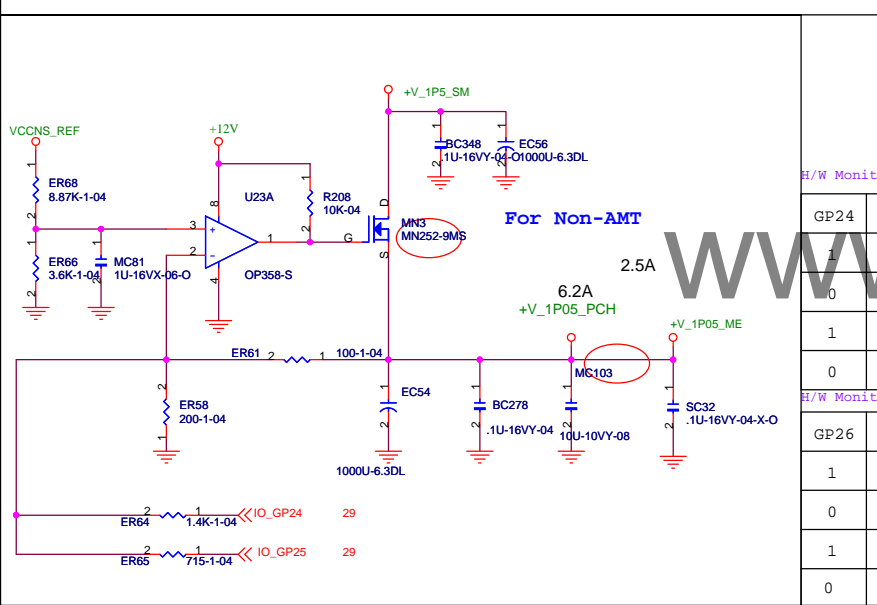
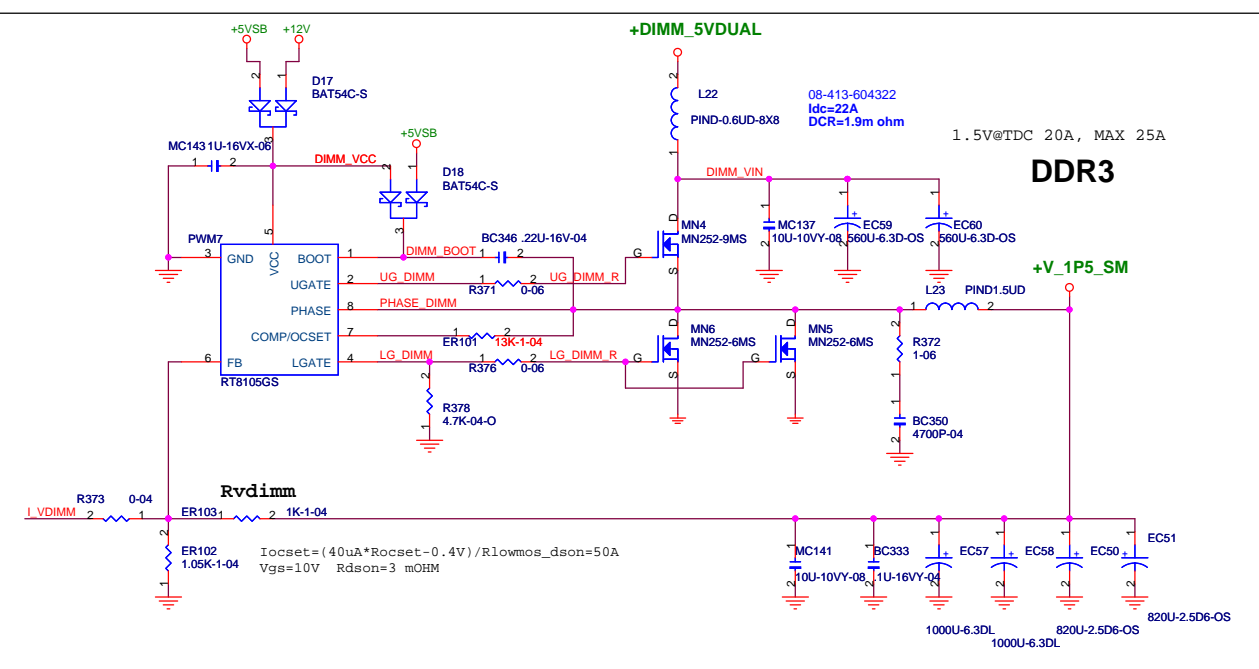
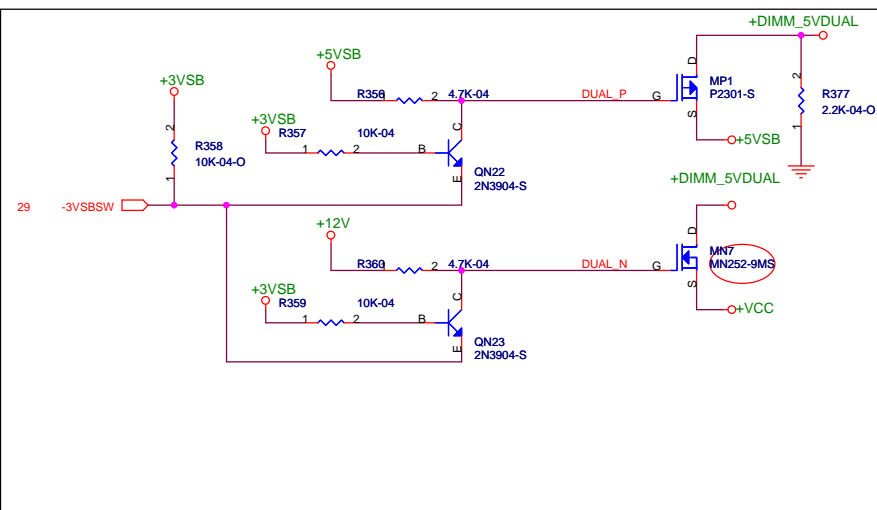


VCCSA Sequence







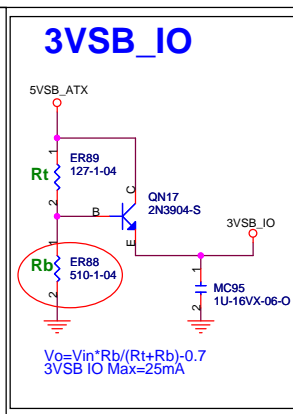


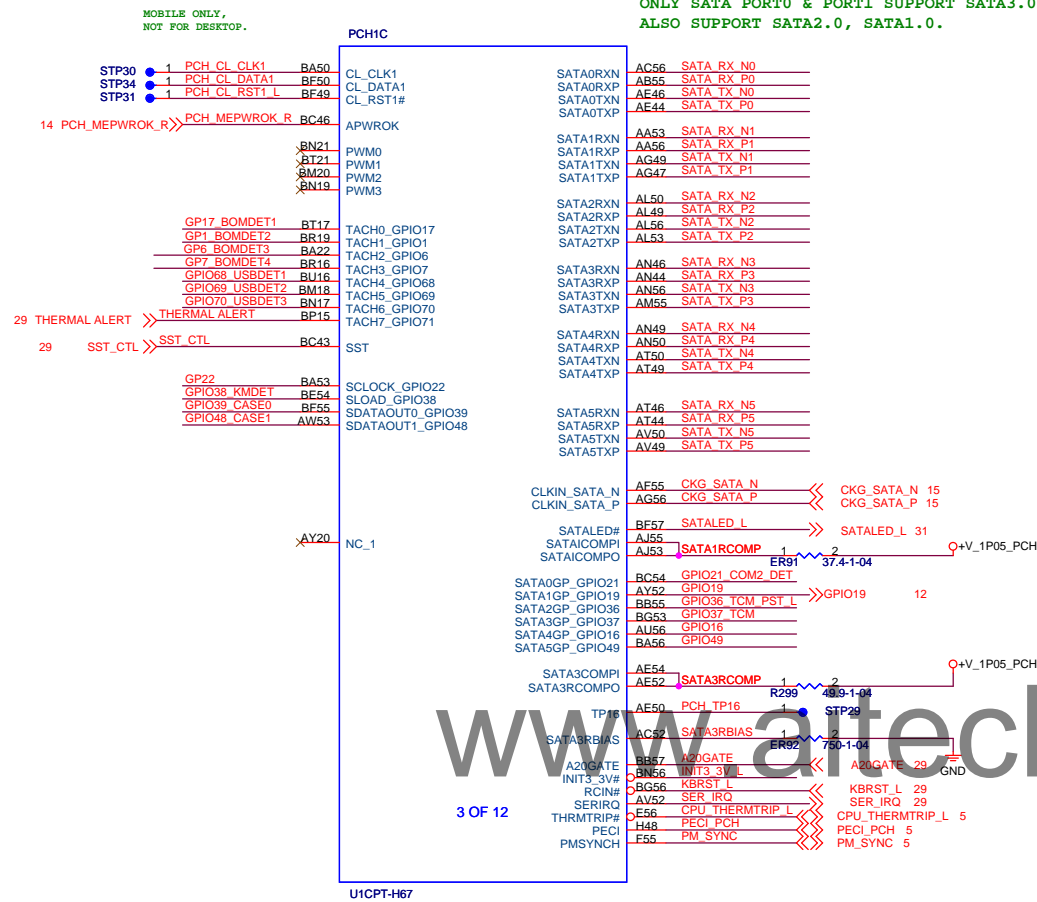
H/W Monitor :1.05V (Traget)

| GP24 | GP25 | PCH |
|------|------|-------|
| 1 | 1 | 1.08V |
| 0 | 1 | 1.13V |
| 1 | 0 | 1.18V |
| 0 | 0 | 1.23V |

H/W Monitor :1.8V (Traget)

| GP26 | GP27 | PLL |
|------|------|-------|
| 1 | 1 | 1.83V |
| 0 | 1 | 1.93V |
| 1 | 0 | 2.02V |
| 0 | 0 | 2.13V |

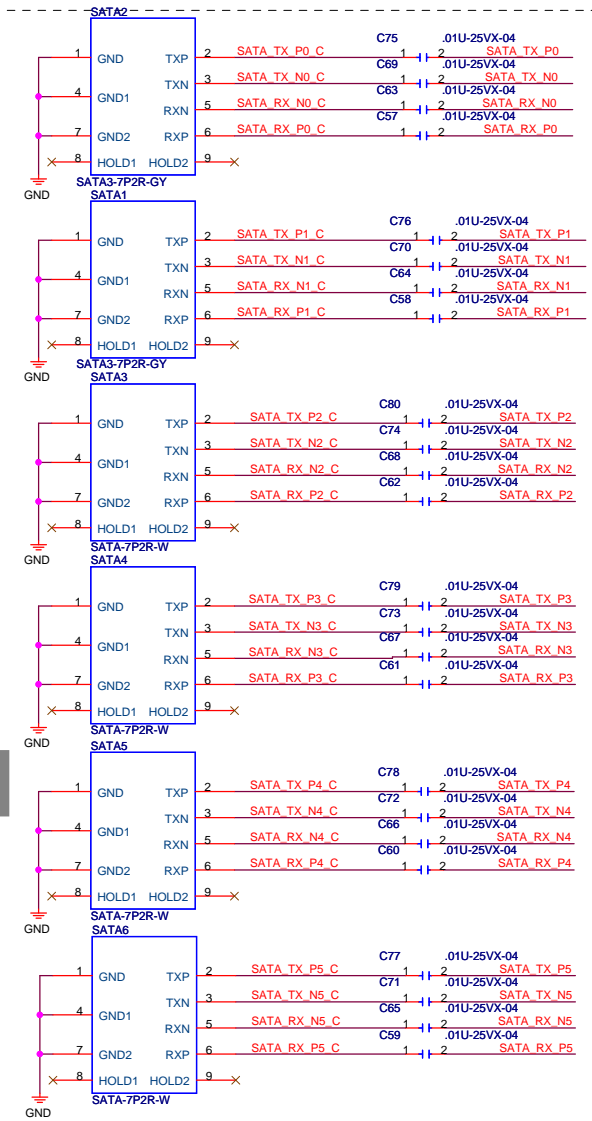
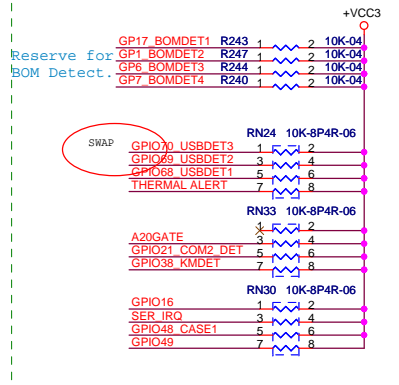




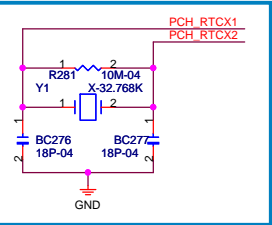
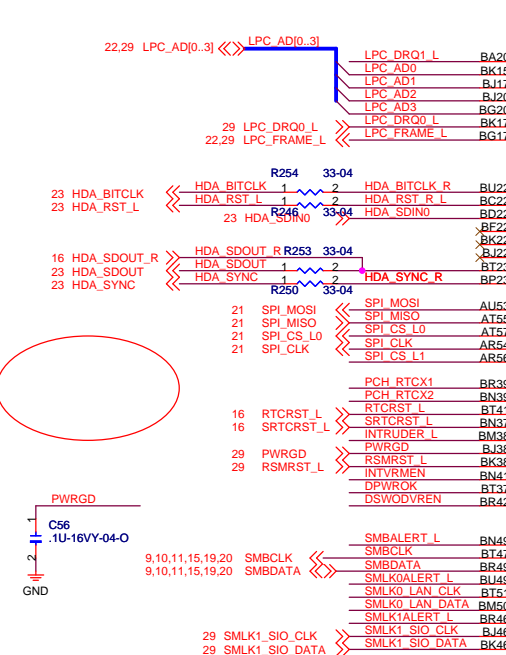
Default GPI set to Pull Up:

GPIO36_TCM_PST_L, GPIO37_TCM:
TCM Header In Enable TCM,
Disable TPM.

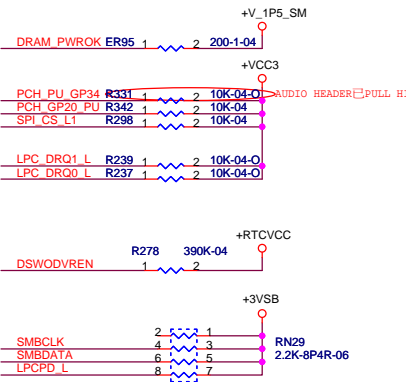
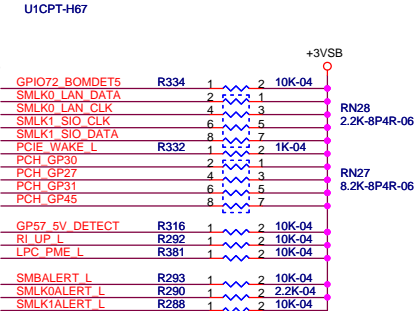
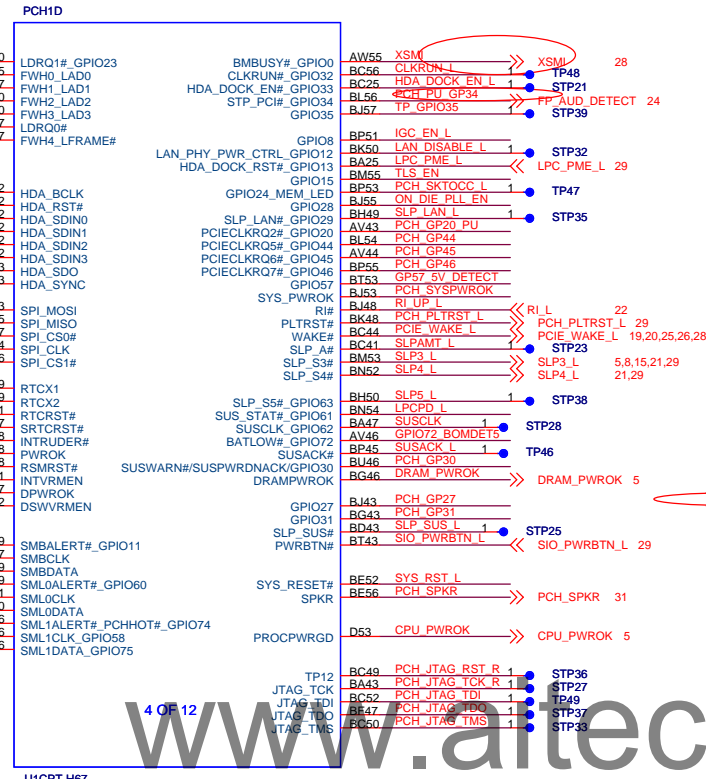
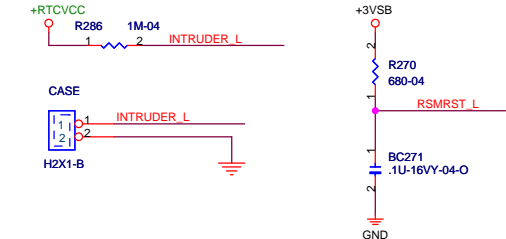
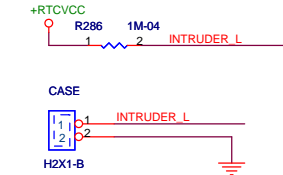
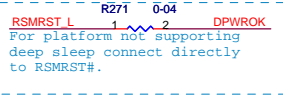
GPIO16, GPIO49:
Reserve for TPM.



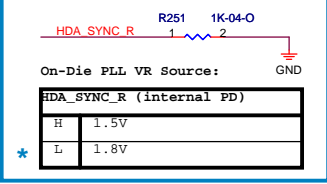
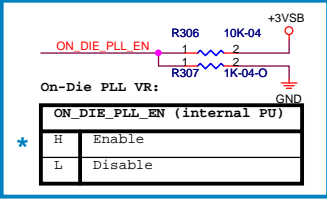
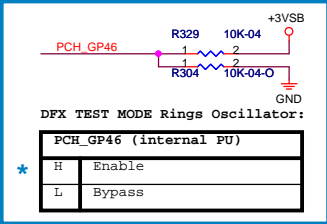
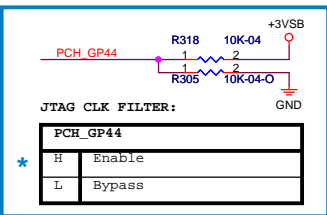
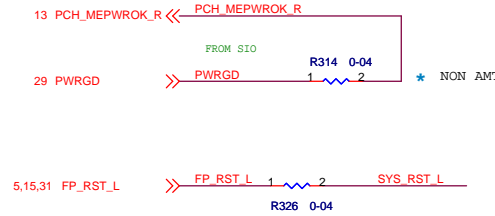
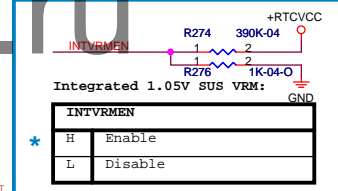
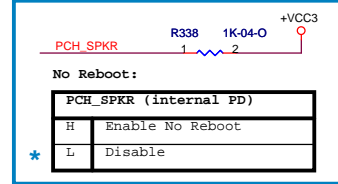
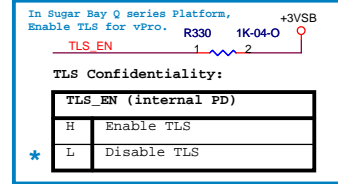
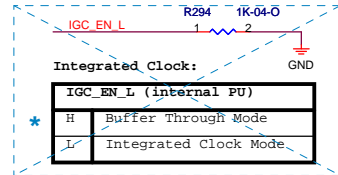
Elitegroup Computer Systems

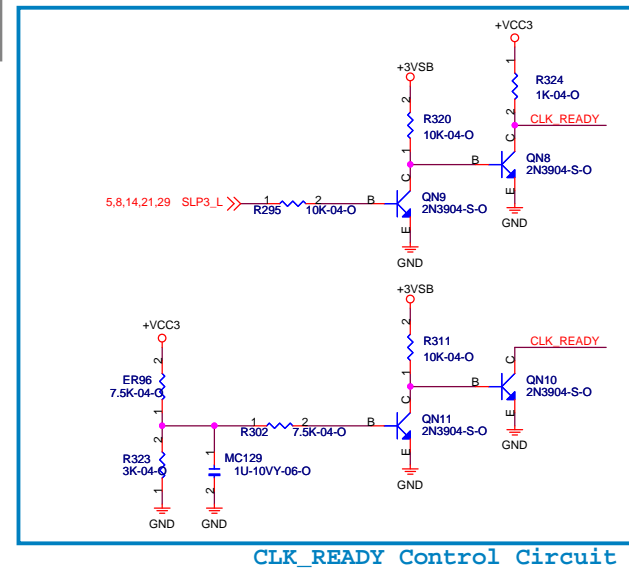
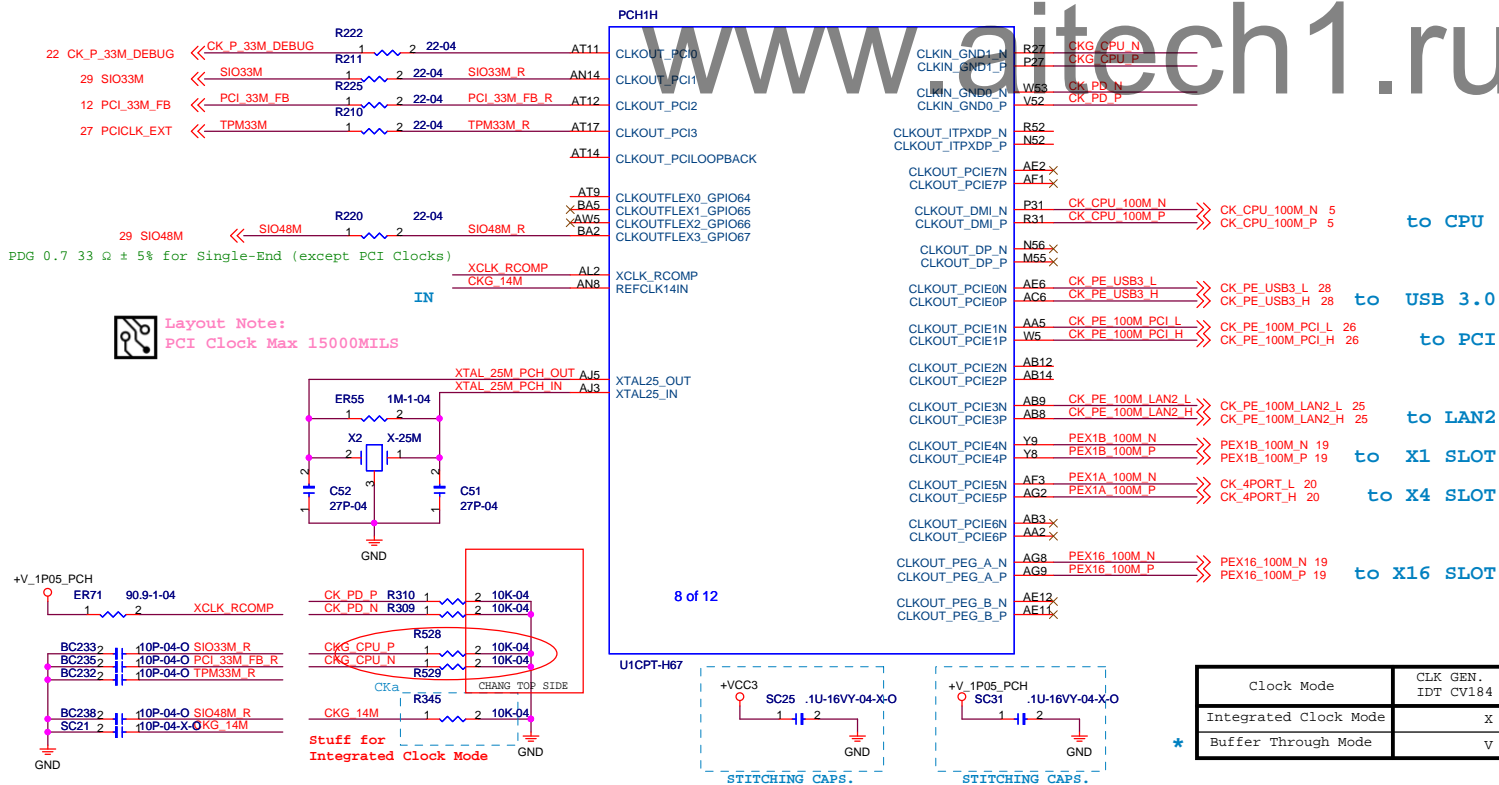
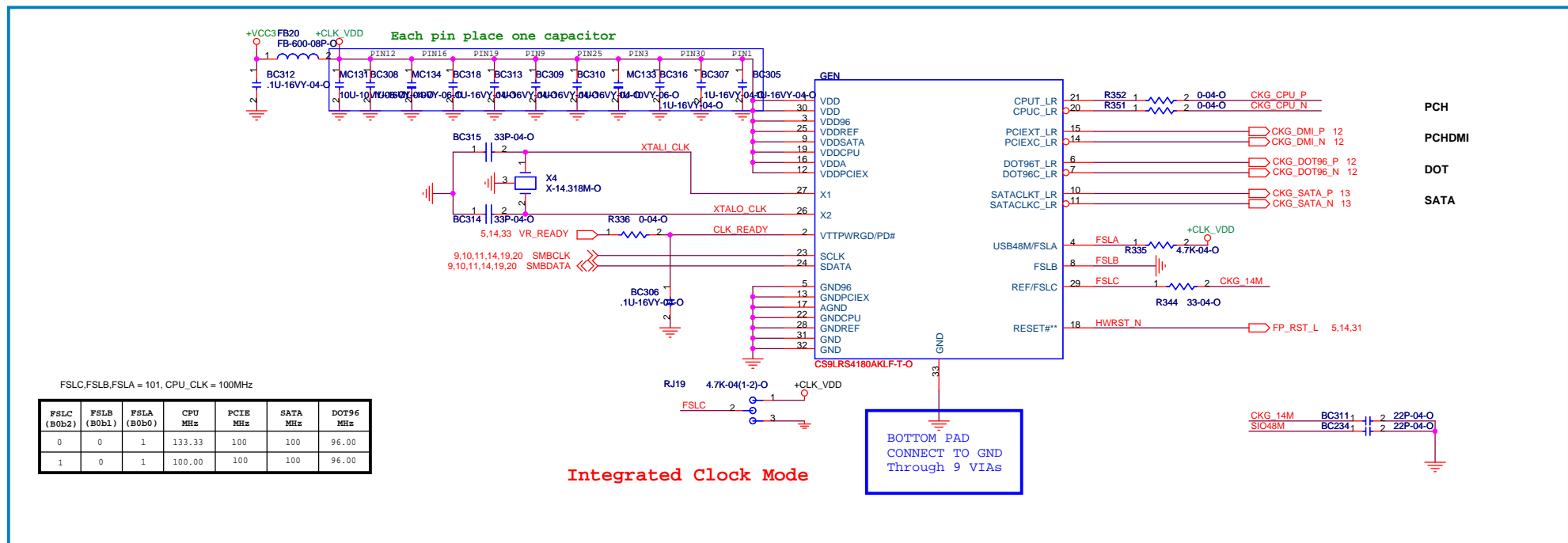


When Deep Sleep not implemented:
1. PCH_GP30, PCH_GP27 need to be Pull Up.
2. VCCDSW3_3 should to be connected to +3VSB.
3. SLP_SUS_L, SUSACK_L left unconnected.
4. SUSWARN# may be used as GPIO30.(Reference to 1.)

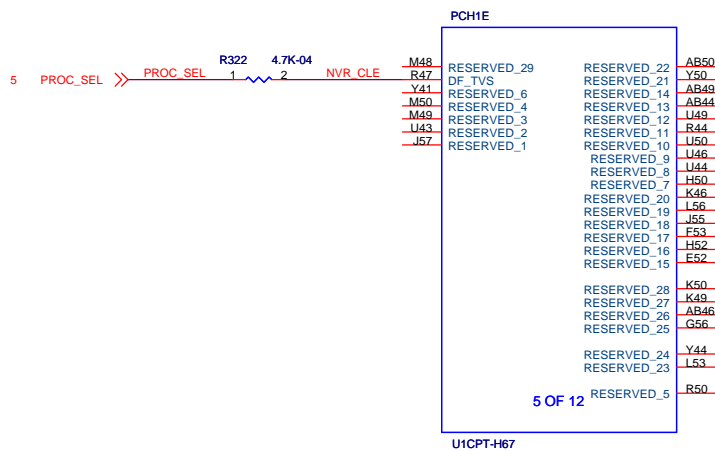


Buffer Through Mode / Integrated Clock Mode have been changed to P/W Strap. Default: Integrated Clock Mode. Doc, Cougar Point Platform Controller Hub (PCH) Family EDS Update V0.7.1





| Clock Mode | CLK GEN. IDT CV184 Circuit. | CKA |
|-----------------------|--------------------------------|-----|
| Integrated Clock Mode | X | V |
| Buffer Through Mode | V | X |



091222 Update!
Terminating unused DC NAND interface:

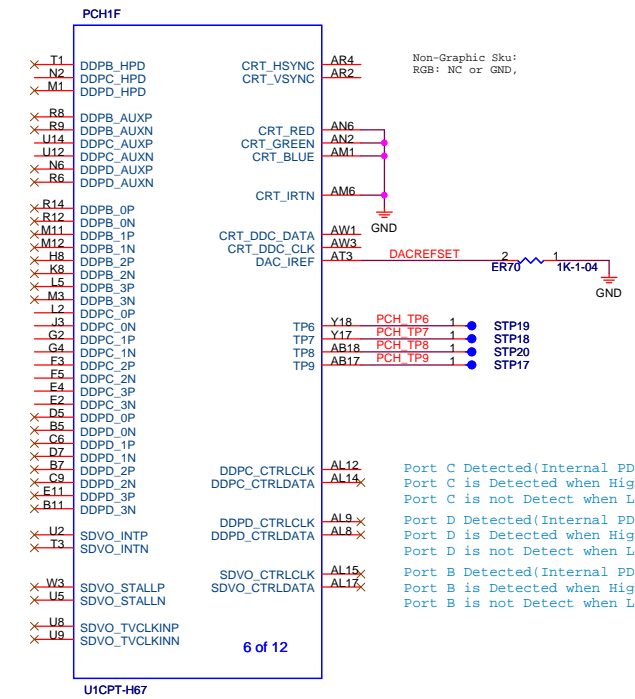
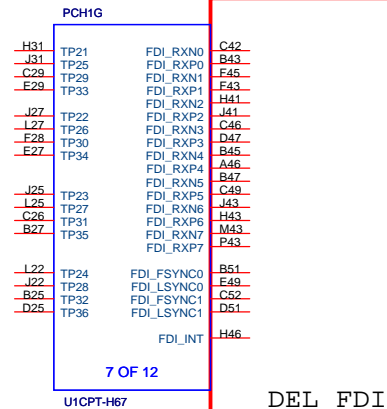
If not implemented, the dual channel NAND interface signals, including NV_RCOMP, can be left as No Connect.

Note:

VCCFNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.

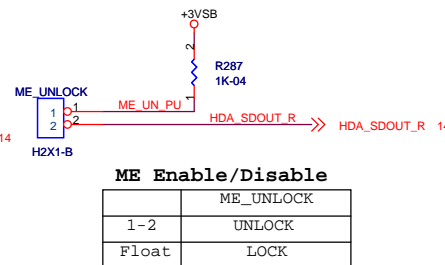
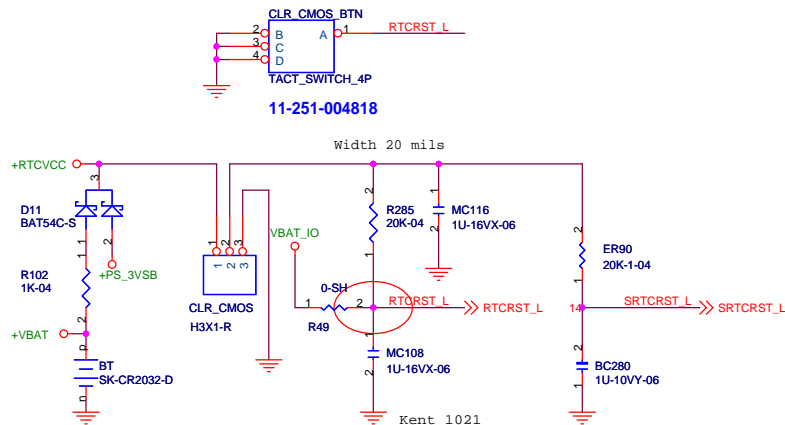
100120 Update!
428880_428880_Cougar_Point_Desktop_Ballout_Mech_Package_Rev1p0.zip:

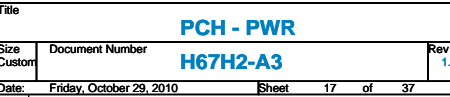
Renamed NV_WE#_CK[0:1], NV_RE#_WRB[0:1], NV_RCOMP, NV_RB#, NV_DQ9 / NV_IO[0:15], NV_DQS[0:1], NV_CE#[0:3], and NV_ALE to Reserved(RSVD).
Renamed NV_CLE to DF_TVS.



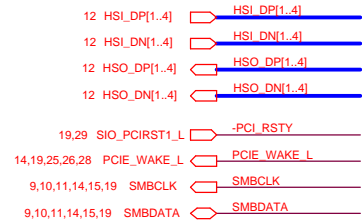
DEL HDMI , DVI , DP , VGA

CLR_CMOS



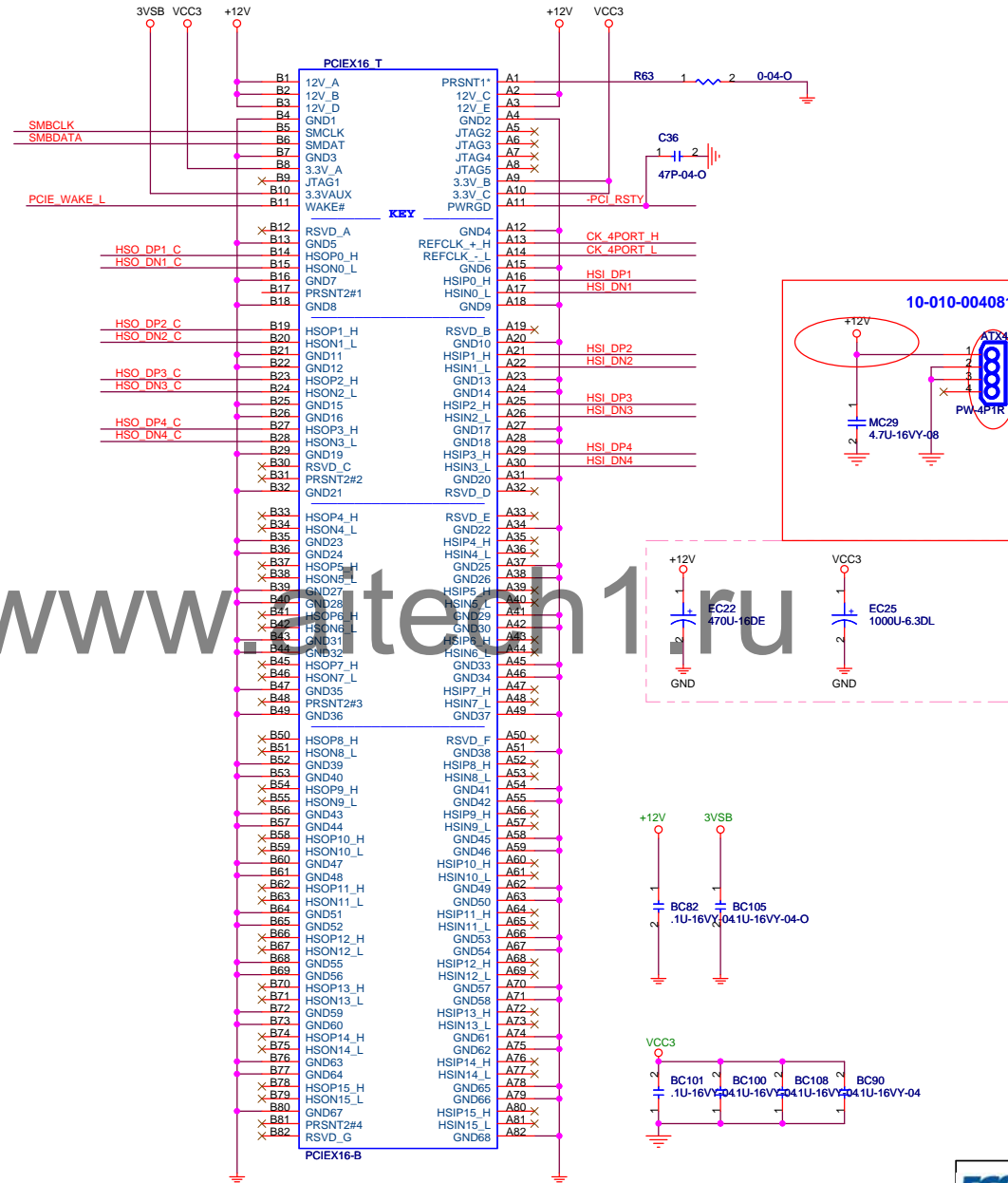


External Connection



| | | | | |
|---------|-----|---|-------------|-----------|
| HSO DN1 | C37 | 1 | 21U-16VX-04 | HSO DN1 C |
| HSO DP1 | C38 | 1 | 21U-16VX-04 | HSO DP1 C |
| HSO DN2 | C41 | 1 | 21U-16VX-04 | HSO DN2 C |
| HSO DP2 | C40 | 1 | 21U-16VX-04 | HSO DP2 C |
| HSO DN3 | C43 | 1 | 21U-16VX-04 | HSO DN3 C |
| HSO DP3 | C42 | 1 | 21U-16VX-04 | HSO DP3 C |
| HSO DN4 | C45 | 1 | 21U-16VX-04 | HSO DN4 C |
| HSO DP4 | C44 | 1 | 21U-16VX-04 | HSO DP4 C |

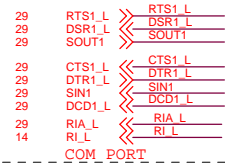
Near chipset



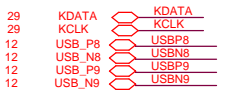
External Connection

del debug card

Debug Card



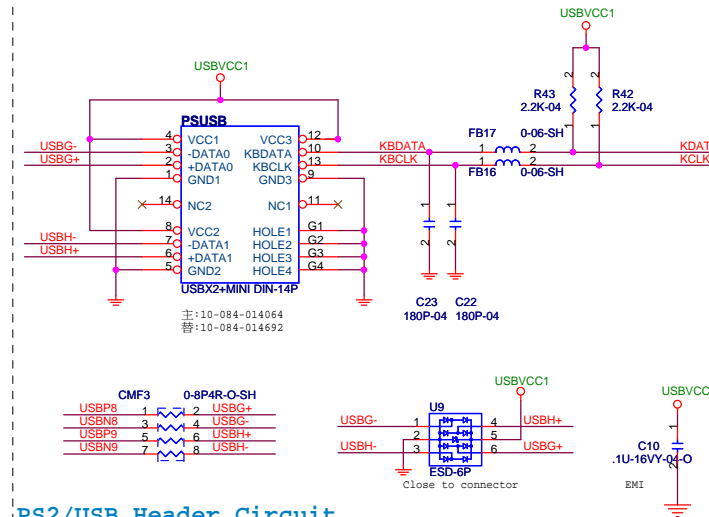
USBVCC1



PS2/USB

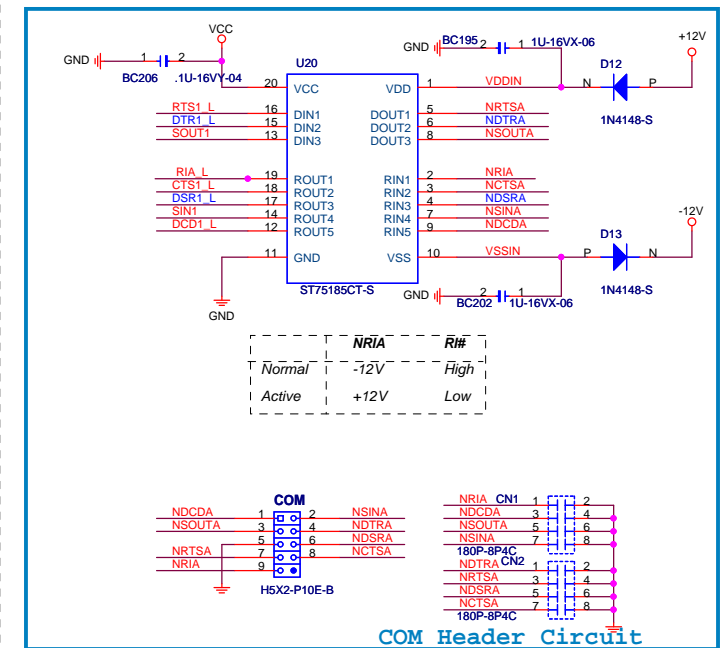
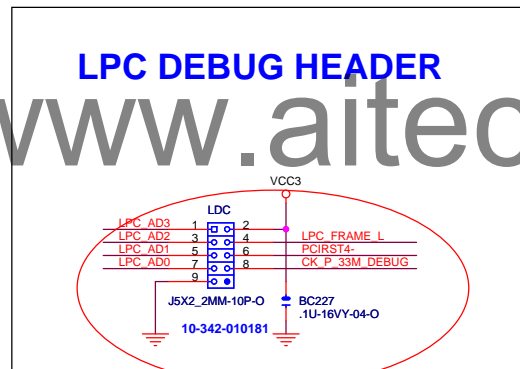
Debug Card

del debug card

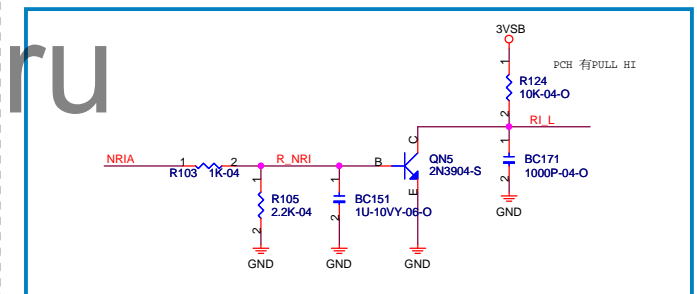


PS2/USB Header Circuit

LPC DEBUG HEADER



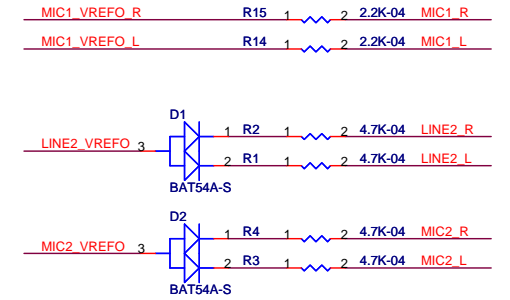
COM Header Circuit



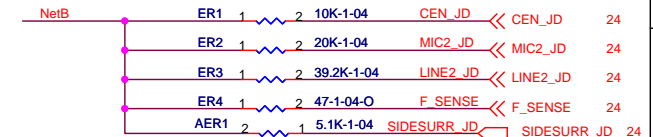
COM RI# Wake Up Circuit

Diagram illustrating the pin configuration for the HDA module:

- 14 HDA_RST_L >> AZ_RST
- 14 HDA_BITCLK >> AZ_BIT_CLK
- 14 HDA_SYNC >> AZ_SYNC
- 14 HDA_SDINO >> AZ_SDATA_IN
- 14 HDA_SDOUT << AZ_SDOUT

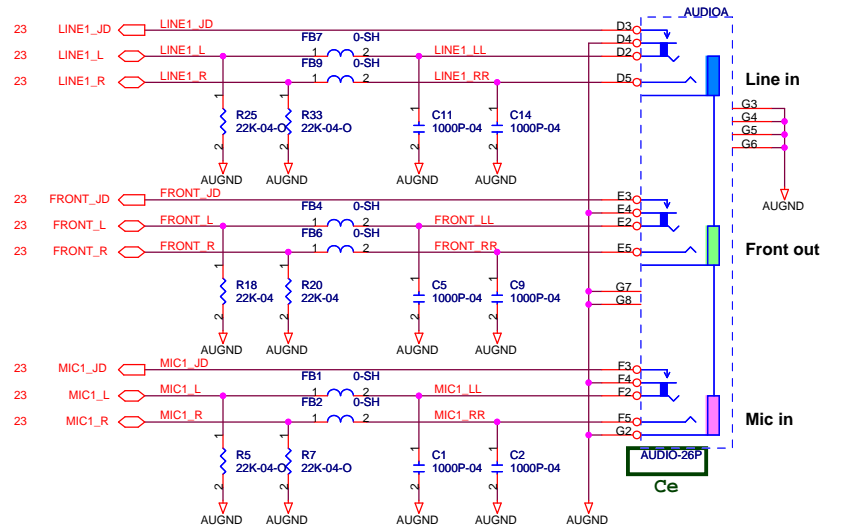


| NetA | Component | Value | Front-End | Back-End | Width |
|------|-----------|------------|-----------|----------|-------|
| NetA | ER12 | 5.1K-1-04 | FRONT_JD | FRONT_JD | 24 |
| | ER13 | 10K-1-04 | LINE1_JD | LINE1_JD | 24 |
| | ER10 | 20K1-04 | MIC1_JD | MIC1_JD | 24 |
| | ER11 | 39.2K-1-04 | SURR_JD | SURR_JD | 24 |

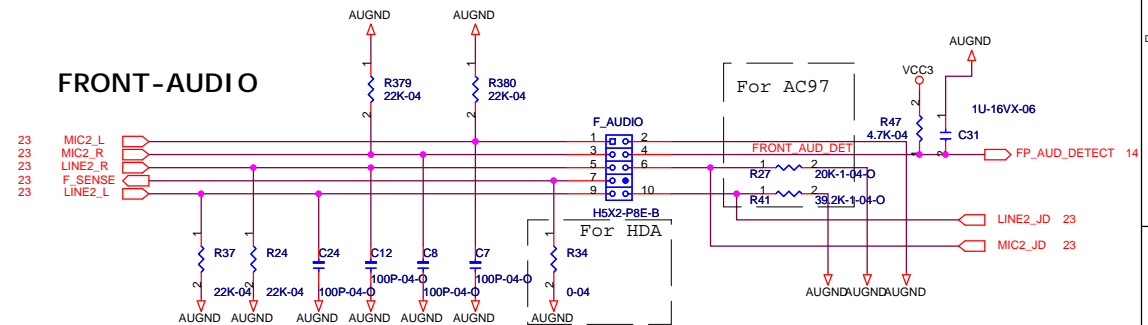


| | | | |
|----------------|--------------------------|-------|----------|
| Title | | | |
| Audio - ALC892 | | | |
| Size | Document Number | Rev | |
| Custom | H67H2-A3 | 1.0 | |
| Date: | Friday, October 29, 2010 | Sheet | 23 of 37 |

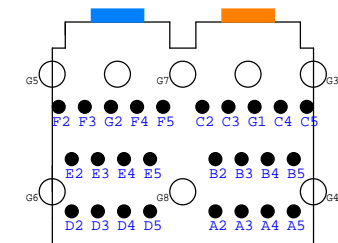
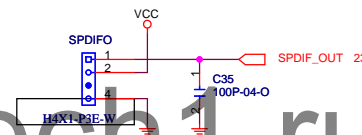
REAR-AUDIO



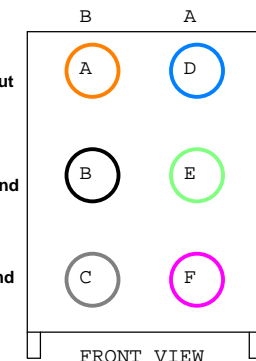
FRONT-AUDIO



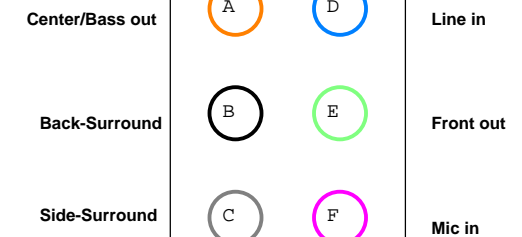
SPDIF-OUT



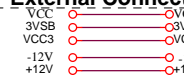
TOP VIEW



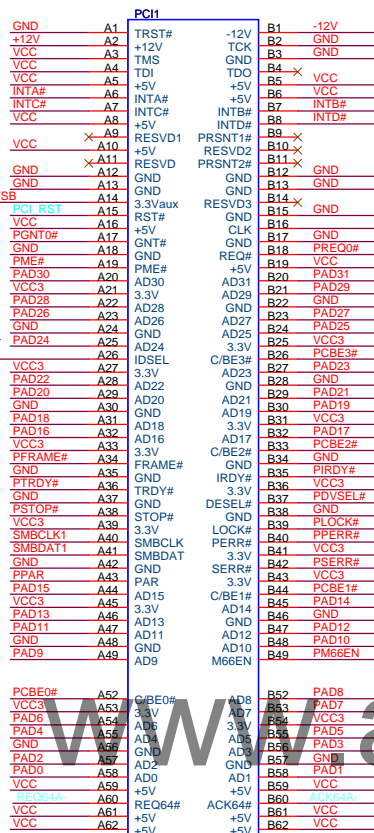
FRONT VIEW



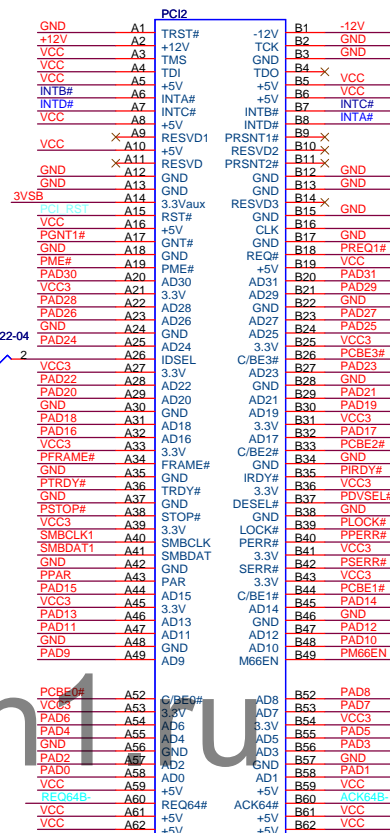
External Connection



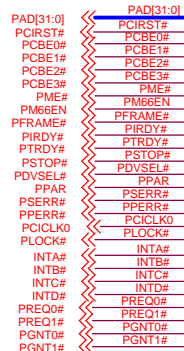
PCI 1



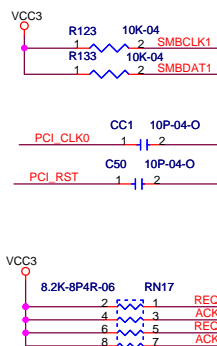
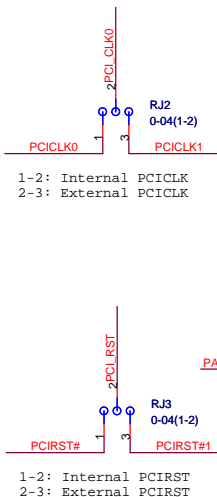
PCI 2



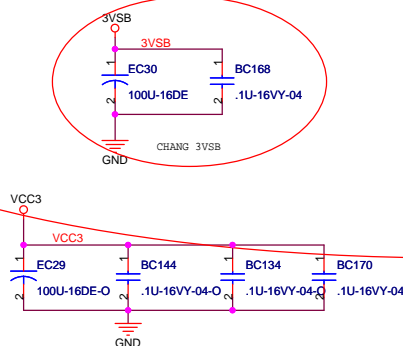
COMMON



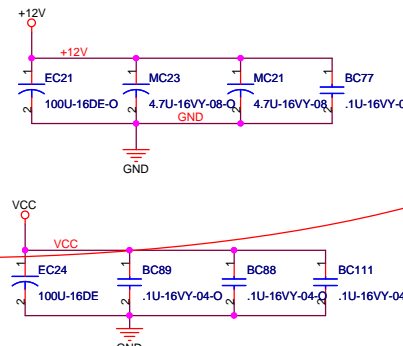
PCI CHIP



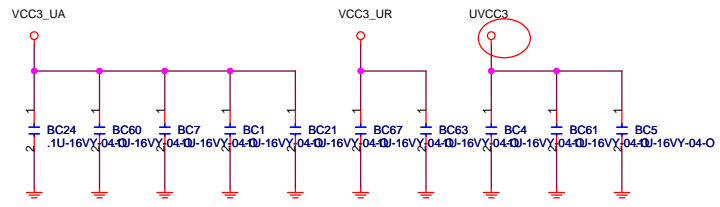
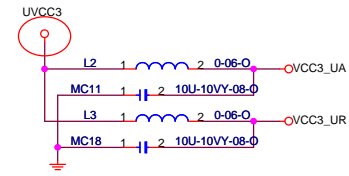
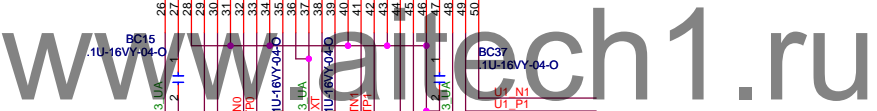
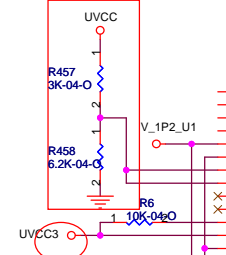
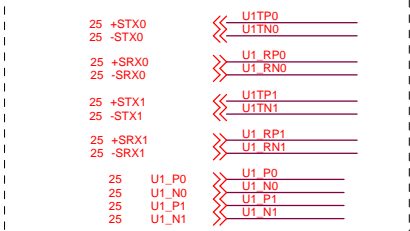
PCI1:REQ0;GNT0 IDSEL:16 INT:ABCD
PCI2:REQ1;GNT1 IDSEL:17 INT:BCDA



精簡零件



| | | | |
|----------------|---------------|-----|-------------|
| 22,25,29 | SIO_PCIRST3_L | >>> | PCIRST3_L |
| 14,19,20,25,26 | PCIE_WAKE_L | >>> | PCIE_WAKE_L |
| 15 | CK_PE_USB3_H | >>> | PCIE_CLK1_P |
| 15 | CK_PE_USB3_L | >>> | PCIE_CLK1_N |
| 12 | USB3_TX_P3 | >>> | PE1X_TP2 |
| 12 | USB3_TX_N3 | >>> | PE1X_TN2 |
| 12 | USB3_RX_P3 | >>> | PE1X_RP2 |
| 12 | USB3_RX_N3 | >>> | PE1X_RN2 |
| 14 | XSMI | >>> | XSMI |



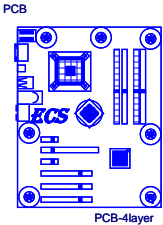
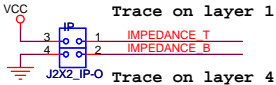
| | Wake up | No Wake up |
|-----|------------|------------|
| U3a | RJ12 (1-2) | RJ12 (2-3) |
| U3b | R385,R382 | R383,R384 |

Wiring diagram for U3a (RJ12) showing D3DET1 connected to pin 2 and 0-04(1-2)-0 connected to pin 1. Pin 3 is connected to ground. A red circle highlights the connection to UVCC3.

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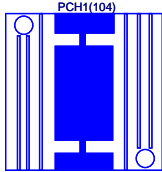
1)Circuit type 1

Layer 1:TOP
Layer 2:PWR
Layer 3:GND
Layer 4:BOTTOM



PCB STACK: L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

20-120-012343



20-120-010851

PN:20-120-010851

CLR_CMOS(1-2)



JP-R

BT(104)



CR2032

Y1(wire)

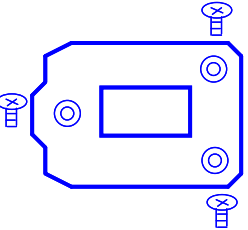
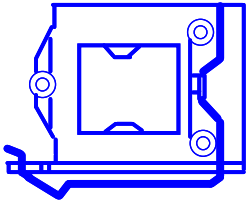


JP-WI-P6.25

11-018-115021 CPU SMD SOCKET
SOCKET.CPU.LGA 1155P SMD.BLACK.PE115527-4041-01F.
LEAD-FREE.FOXCONN

20-800-004711 CPU SOCKET STEEL
SUBASSY.STEEL.LGA 1156P.W/
BACK PLATE.PT44A11-6401.LEAD-FREE(RoHS).FOXCONN

CPU1(104)
CPU_SUBASSY_STEEL



01D201-000060 PCH E50



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Title

Size
Custom

Document Number

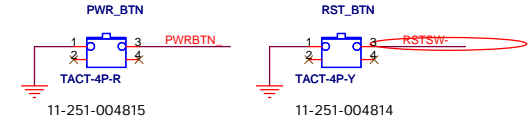
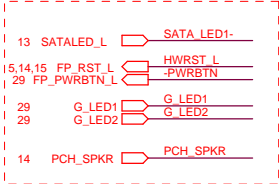
H67H2-A3

Rev
1.0

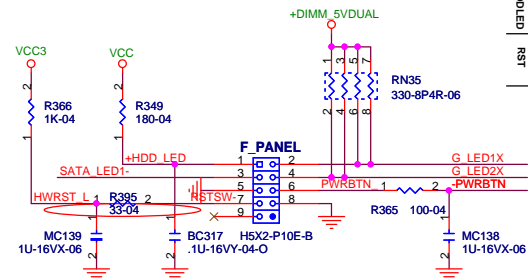
Date: Friday, October 29, 2010

Sheet 30 of 37

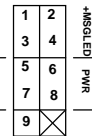
External Connection



FRONT PANEL

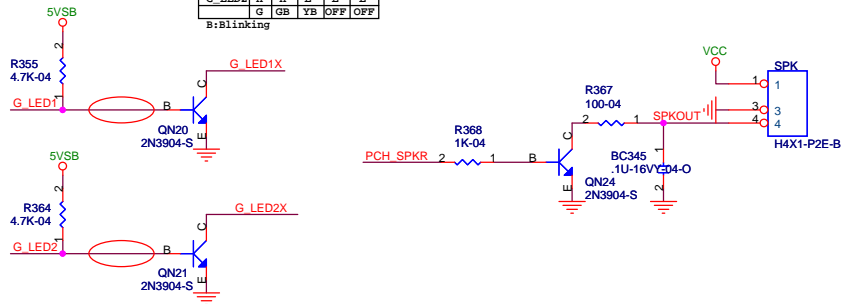


F. PANEL



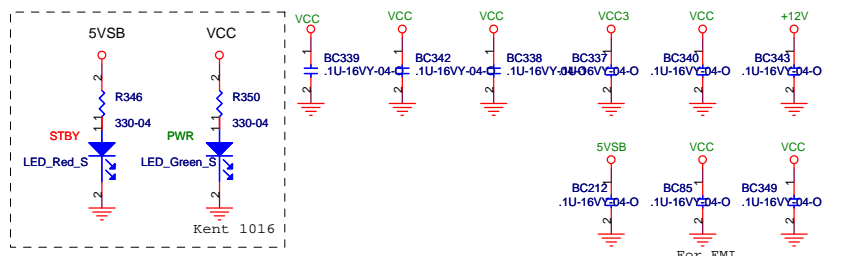
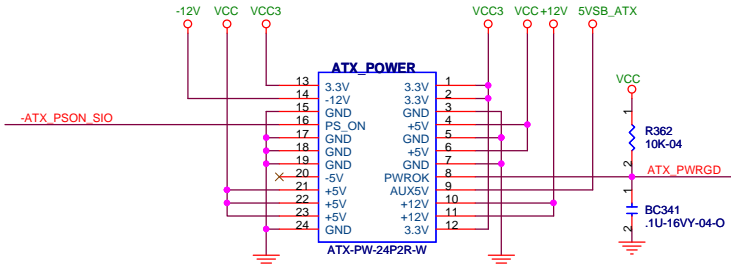
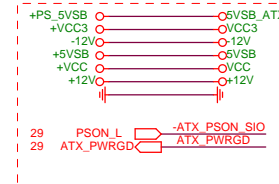
| | | | | |
|--------|----|-----|-----|-----|
| S0 | S1 | S3 | S4 | S5 |
| G LED1 | L | B | B | L |
| G LED2 | H | H | L | L |
| G GB | YB | OFF | OFF | OFF |

B: Blinking



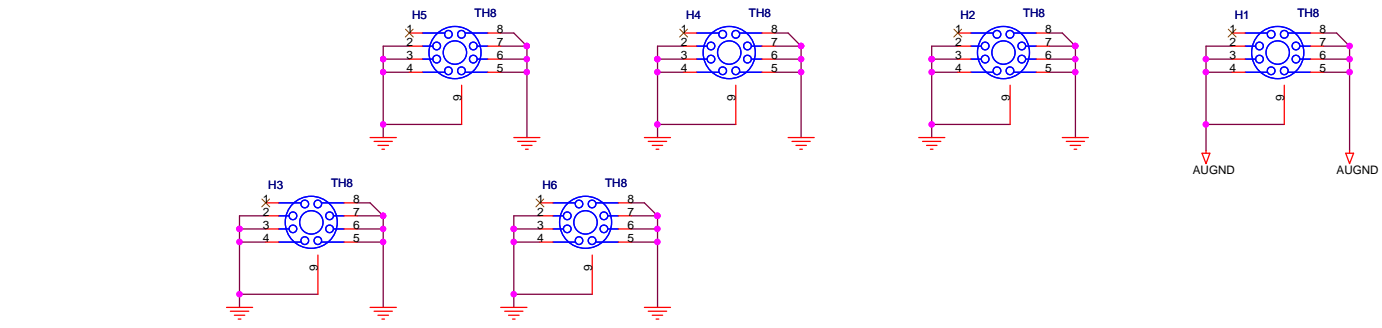
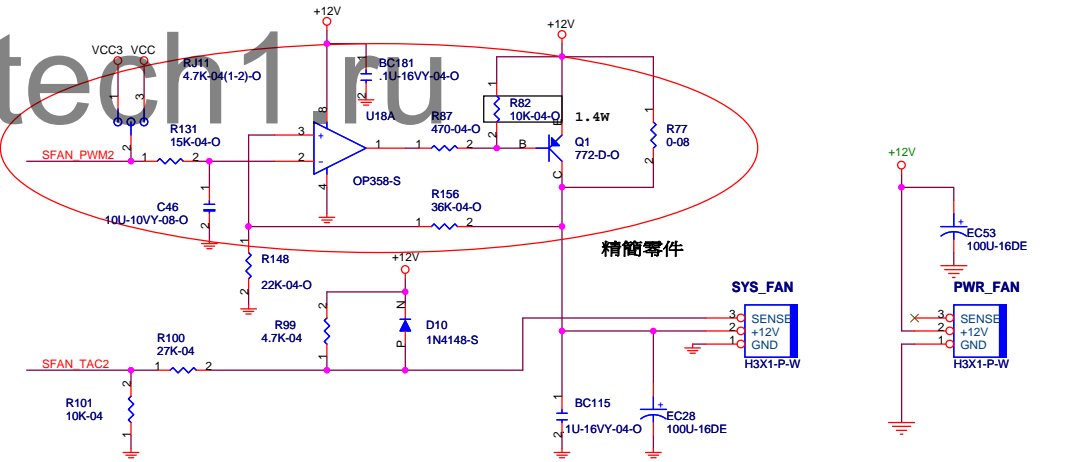
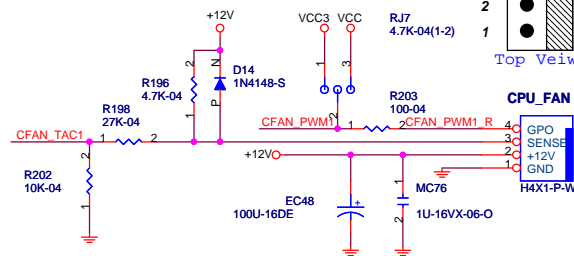
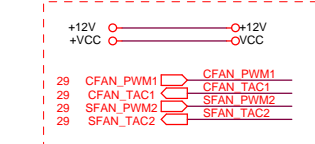
POWER CONNECTOR

External Connection



FAN

External Connection



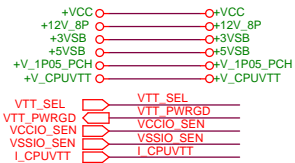
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Front Panel,FAN,PowerConn

Size Custom Document Number
H67H2-A3

Date: Friday, October 29, 2010 Sheet 31 of 37

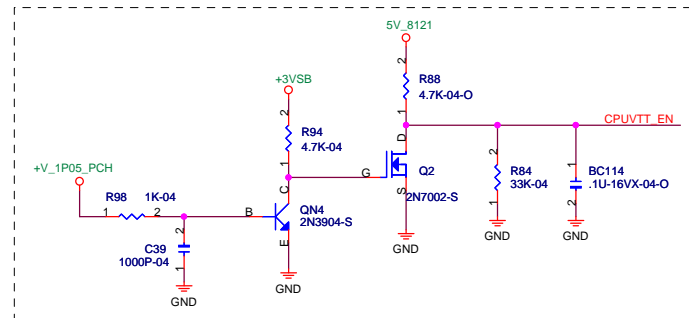
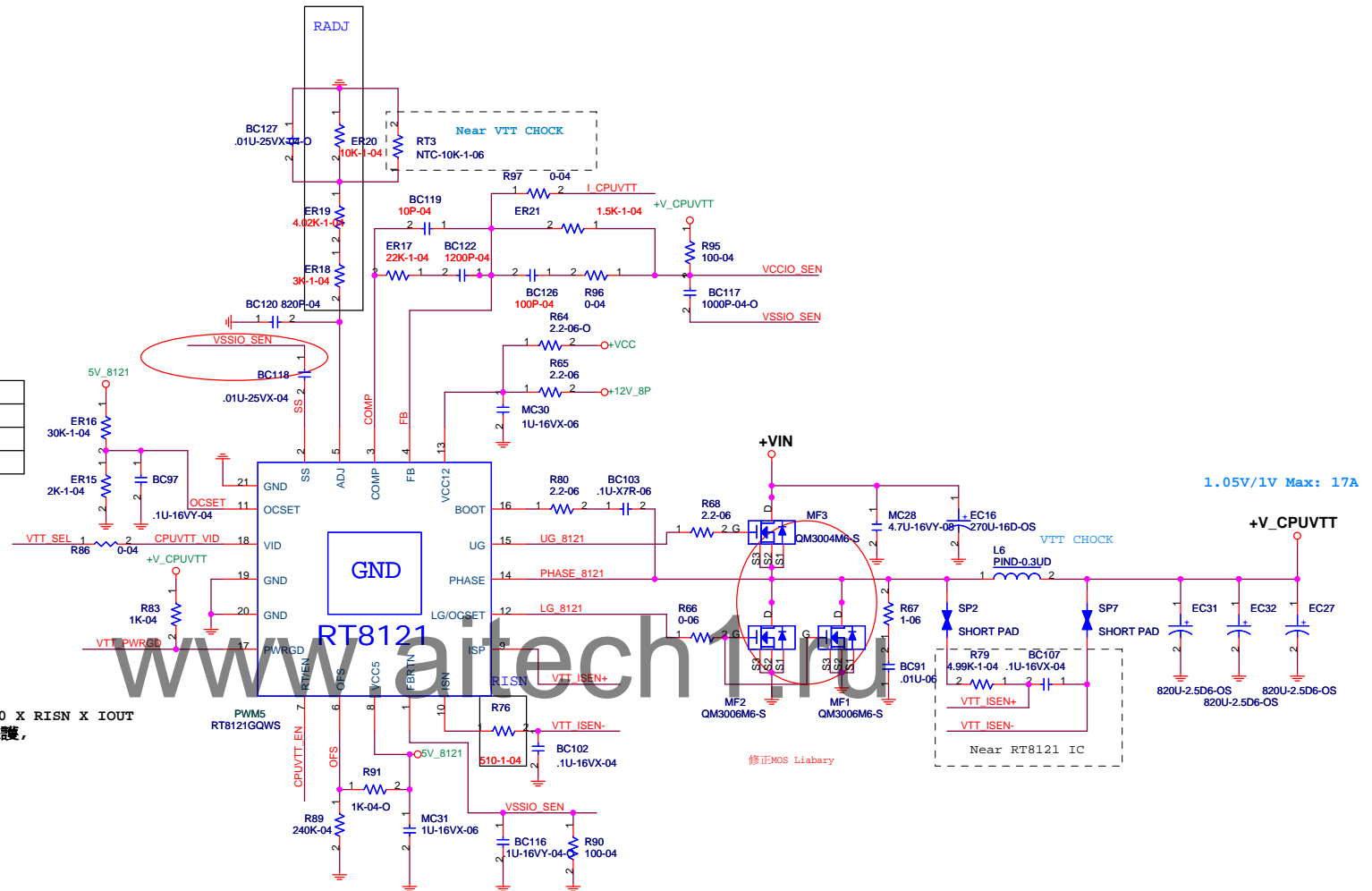
Rev
1.0

External Connection

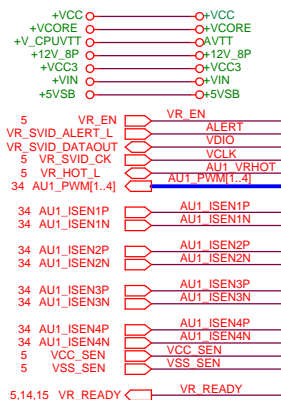


| VCCIO voltage selection | |
|-------------------------|----------|
| VTT_SEL | V_CPUVTT |
| low | 1V |
| high | 1.05V |

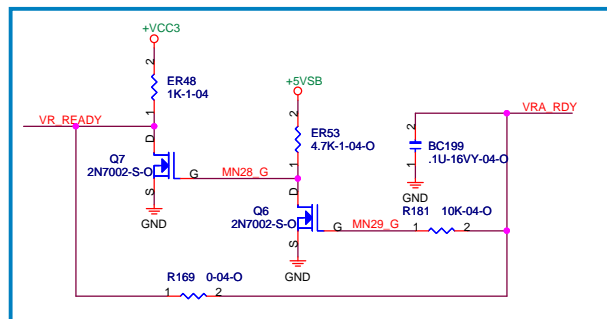
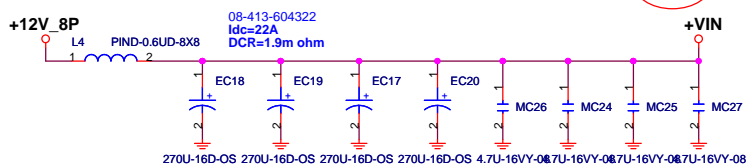
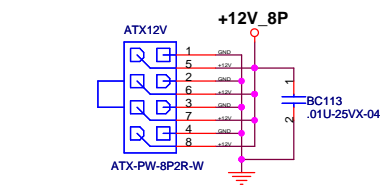
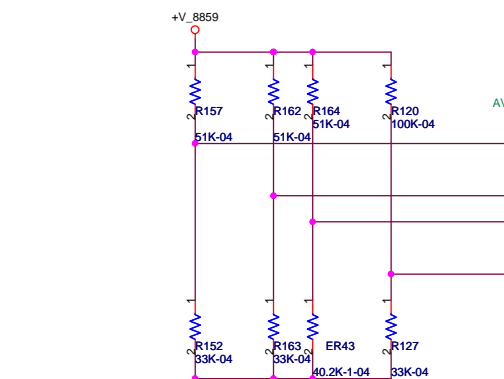
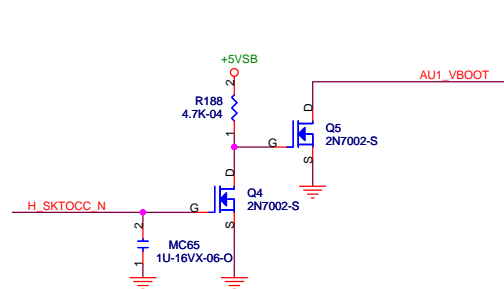
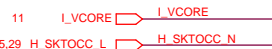
$V_{ADJ} = LL \times I_{OUT} = DCR \times RADJ / 20 \times R_{ISN} \times I_{OUT}$
 OCP設定方式就是VADJ > VOCSET 時保護，



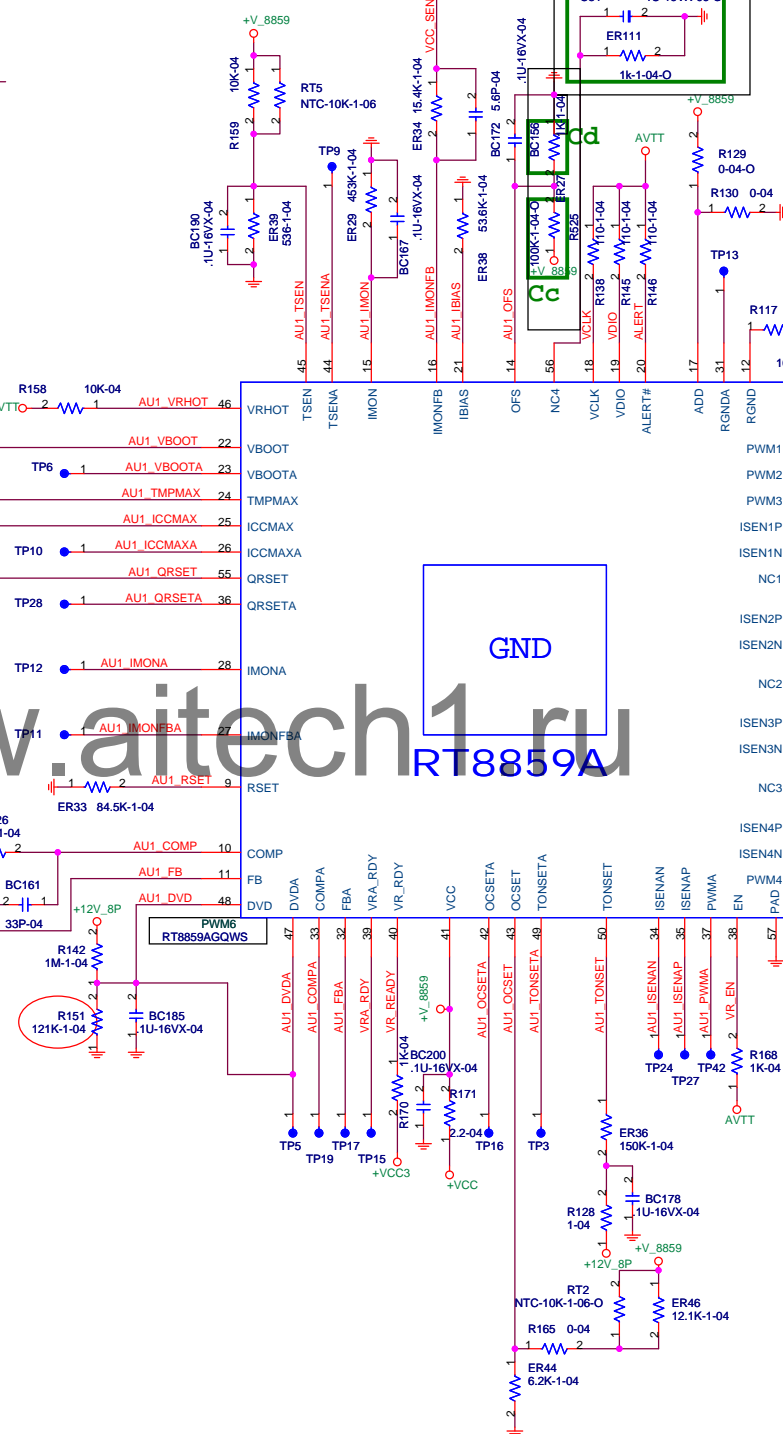
External Connection



DEL VAXG

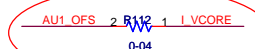


For VR_READY Power On Sequence

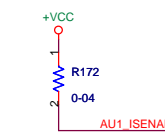
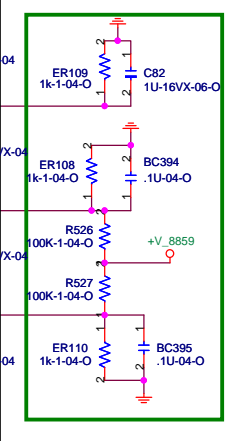


BOM Difference

| | RT8859A | RT8859M |
|----|----------|---------|
| Ca | X | V |
| Cb | X | V |
| Cc | X | V |
| Cd | 402-1-04 | 1k-1-04 |



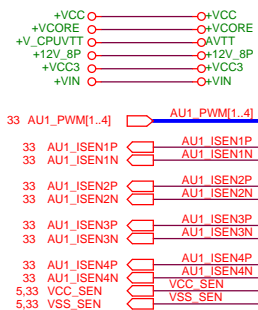
Cb



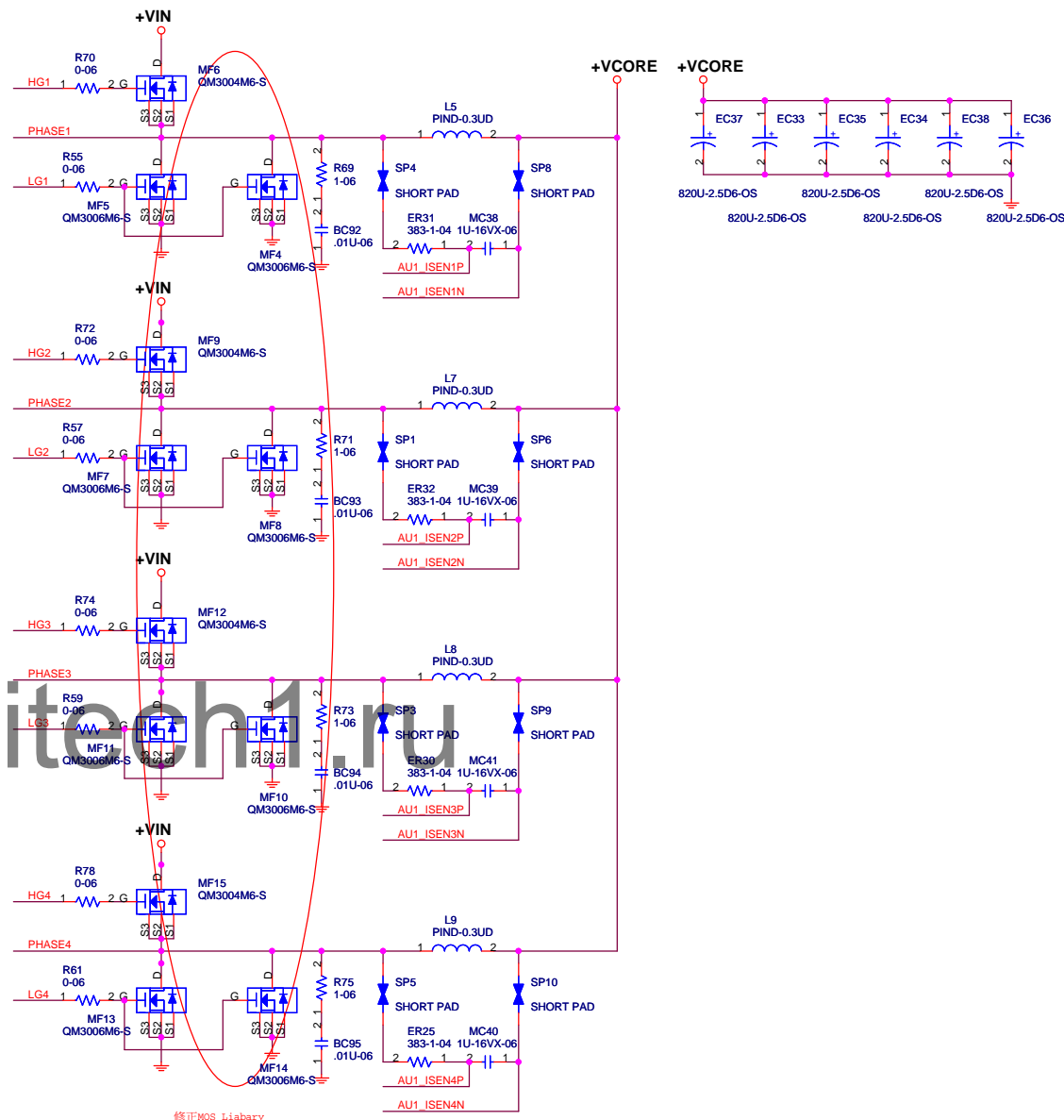
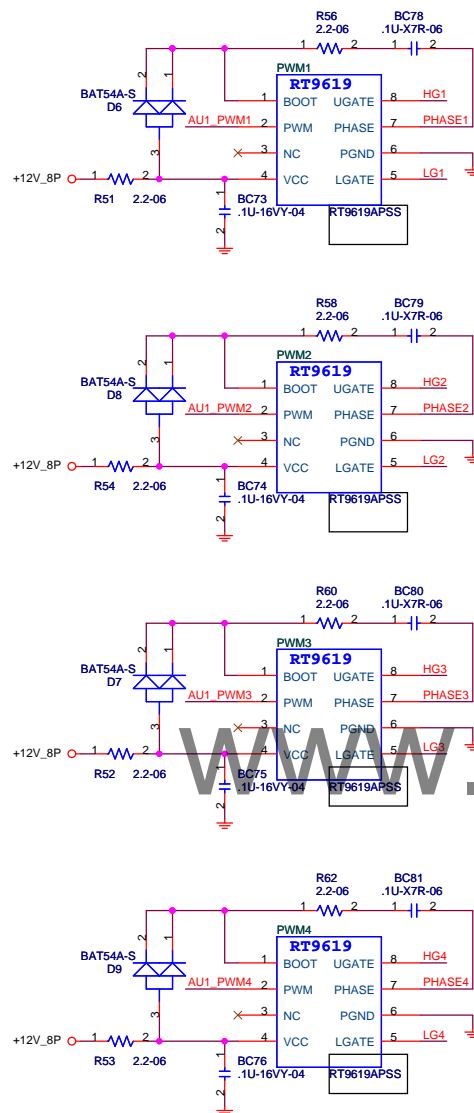
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| | |
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| Title | DC/DC VCORE/VAXG RT8859A |
| Size | Document Number |
| Custom | H67H2-A3 |
| Date | Saturday, November 06, 2010 |
| Sheet | 33 of 37 |

External Connection



DEL VAXG



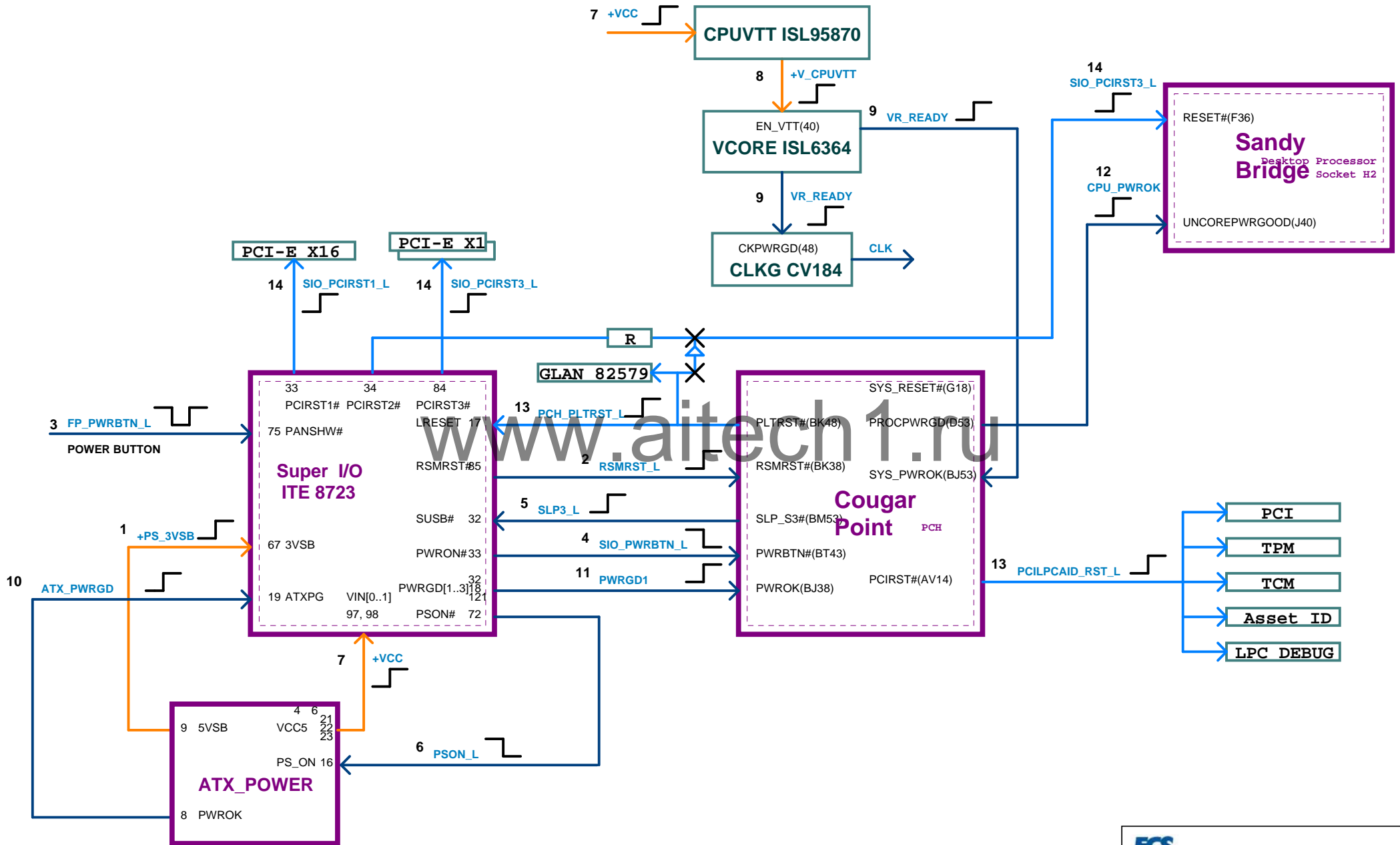
修正MOS Libary

DEL VAXG



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| Title | | DC/DC VCORE/VAXG RT9619 |
| Size | Document Number | H67H2-A3 |
| Custom | Rev | 1.0 |
| Date: | Saturday, November 06, 2010 | Sheet 34 of 37 |



NOTE:

Sugar Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option

